5 Packet Switching

5-1 Research and Development of 160 Gbit/s/port Optical Packet Switch Prototype and Related Technologies

WADA Naoya

We have developed optical packet switch (OPS) prototype with optical code label processing, optical switching, optical buffering, and electronic scheduling to improve drastically the switching performance of optical packets in photonic network nodes. 160 Gbit/s/port OPS prototype is developed by introduction of 25 Gchip/s narrow-band optical code label processing and optical buffering with noise reduction function.

A novel packet bit error rate (BER) and loss real-time measurement method and system for 40 Gbit/s variable-length packets has been proposed. Packet BER and loss real-time measurement with various conditions is experimentally demonstrated by using proposed measurement system and OPS system. By using the proposed system, only the payload data part of packet and burst data, which varies in interval time and packet length, is evaluated. Packet BER and loss real-time measurement with 160 Gbit/s variable-length OPS, OTDM-MUX/DEMUX, and 10 Gbit/s preamble free optical packet 3R receiver are experimentally demonstrated.

Finally, integral demonstration by using 160 Gbit/s/port OPS prototype with optical buffer, packet BER evaluation system, and OTDM-MUX/DEMUX system with 160 Gbit/s and 10 Gbit/s light signal is reported.

Keywords
Photonic network, Optical packet switching, Narrow-band optical code label processing, Optical buffering, 160 Gbit/s/port optical packet switch prototype, Variable-length optical packet, Packet BER evaluation, Packet-loss evaluation, Optical packet receiver

1 Introduction

In recent years, numerous optical packet switch (OPS) systems have been developed, as researchers pursue the significant advantages such systems have to offer, such as high scalability, fine granularity, and ultra-high-speed hopping[1]-[5]. Last year, our group proposed a narrow-band optical code (OC) label processing function for *20-to-160-Gbit/s* multi-channel rate OPS systems[6]. A validation experiment was subsequently carried out to test 160-Gbit/s × 2 WDM fixed-length optical packet switching for transmissions exceeding 50 km, based on the proposed method[6]. However, a comprehensive performance validation experiment on prototypes equipped with an optical packet contention resolution function (based on optical buffering and electronic scheduling), etc., has yet to be conducted.

On the other hand, real-time evaluation of the packet-bit-error rate (BER) and loss is also extremely important in any OPS network.

Thus, a real-time measurement system has been contrived for packet BER and loss using 10-Gbit/s optical packet 3R receivers[8] that require no preamble (i.e., a set of bits sacrificed at the head of optical packets); this system has additionally been subject to experimental validation[7]. However, this system is capable only of measuring the payload data section of the packet and a burst stream with constantly fluctuating packet-interval times, leaving the problem of measuring packet streams having variable-length payload data sections.

This paper presents a novel 40-Gbit/s variable-length packet evaluation system capable of real-time measurement of packet BER and loss for variable-length asynchronous-arrival random packets. Using this system, a validation experiment was performed to test the generation and label switching of 160-Gbit/s OTDM variable-length random packets by narrow-band OC label processing. The paper also addresses real-time measurement of BER and loss for variable-length packets combining OTDM-MUX/DEMUX and optical packet 3R receivers, in order to verify the effectiveness of the proposed method.

Next, these systems were used to conduct a comprehensive performance test of the 160-Gbit/s/port optical switch prototype based on narrow-band OC label processing, optical switching, optical buffering, electronic scheduling, OTDM-MUX/DEMUX, and real-time measurements of packet BER and loss, as part of efforts to examine the feasibility of an ultra-high-speed OPS system.

2 Real-time evaluation system for 40-Gbit/s variable-length packets

Real-time measurement of packet BER and loss are highly important issues in OPS network development. As shown in Fig.1(a), a conventional continuous-system BER evaluation system can be used to perform BER evaluation even for packet-type data, at least within a simple transmission configuration. However, it is impossible to perform BER evaluation using conventional systems when part of the packet is lost or is merged during the packet-switching process [Fig.1(b)], or when the packet interval changes dynamically due to buffering [Fig.1(c)], or when the ordering of the packets are disrupted by routing [Fig.1(d)]. Nor in such cases is it possible to conduct real-time measurement of packet loss.

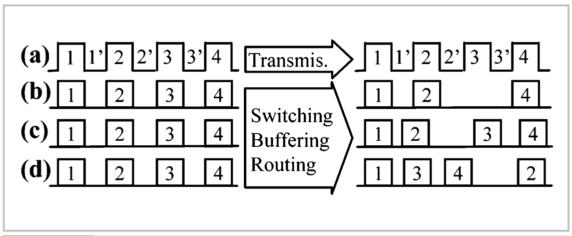

Fig.1 *Example of transformation of the packet data train*

Figure 2 shows a block diagram of a real-time measurement system for 40-Gbit/s variable-length packet BER and loss. After E/O conversion by the optical packet 3R receiver[8], the packet data are demuxed and input to the measurement system, which consists of software for pattern editing and error analysis and a variable-length packet error evaluation section. The error evaluation section consists of five subsections (frame detection, realignment, sequence and payload-length detection, reference pattern and BER detection, and packet-loss count) and a CPU. The results of error evaluation are output to the CPU and processed and displayed by the PC.

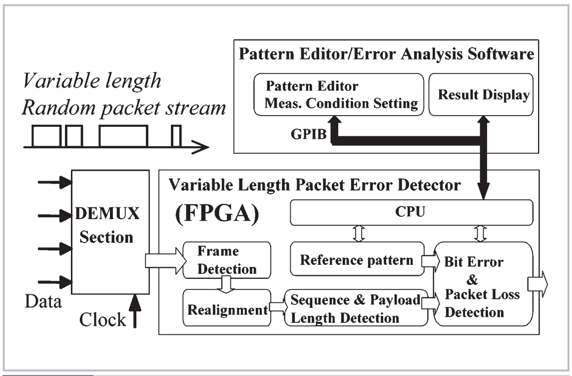

Fig.2 *Block diagram of real-time BER & loss evaluation unit for 40-Gbit/s packet*

One of the features of this system is that all five functions of the error evaluation section are packaged in hardware form within an FPGA. This allows the system to perform evaluation at significantly higher speeds relative to software-packaged evaluation systems, and also allows the system to perform real-time measurements of optical packet data input at 40-Gbit/s.

Figure 3(a) is a block diagram of the FPGA. This error-evaluation section is capable of real-time measurement of data up to a total volume of 40-Gbit/s. To enable measurement even when there is a change in package sequence, internal parallel processing and error detection is executed for each packet. Data for which frames have been detected are aligned in the proper DEMUX sequence by realignment sections A and B. The sequence information (packet number and payload length) is detected from the realigned packet data. The variable-length payload data are extracted from the realigned input data based on the variable-length gate pulse, which is itself controlled by the detected payload-length information. Payload data corresponding to the detected packet number is read from RAM and compared to the variable-length payload data extracted by the BER detection section. Packet-loss measurement is carried out through threshold evaluation of the packets for which packet loss can and cannot be detected[7]. An external view of the developed real-time variable-length packet measurement system is presented in Fig.3(b).

Figures 4(a) and (b) present the architecture and an external view of the preamble-free 10-Gbit/s optical packet 3R receiver prototype, respectively[8]. The basic elements of this receiver are the UTC-PD, D-FF, EX-NOR, phase shifter, and low-jitter gated VCO. This prototype is capable of performing clock reproduction in less than 100 ps even for packet data with randomly fluctuating interval times of several tens to several tens of thousands of bits, when the packet data has an average packet length on the Internet of 500 bytes/s 10 Gbit/s[8].

3 160-Gbits/s/port variable-length OPS experiment

Figure 5 shows a block diagram of the experimental system for real-time evaluation of packet BER and loss for 160-Gbit/s/port variable-length packet switching using narrow-band OC label processing. The system consists of a packet-pulse generator (PPG), an optical packet transmitter, a 10-to-160-Gbit/s OTDM multiplexer, a narrow-band OC label processor, a variable-length optical switch, a 160-to-10-Gbit/s OTDM demultiplexer, an optical packet 3R receiver, and a variable-length packet error-evaluation unit.

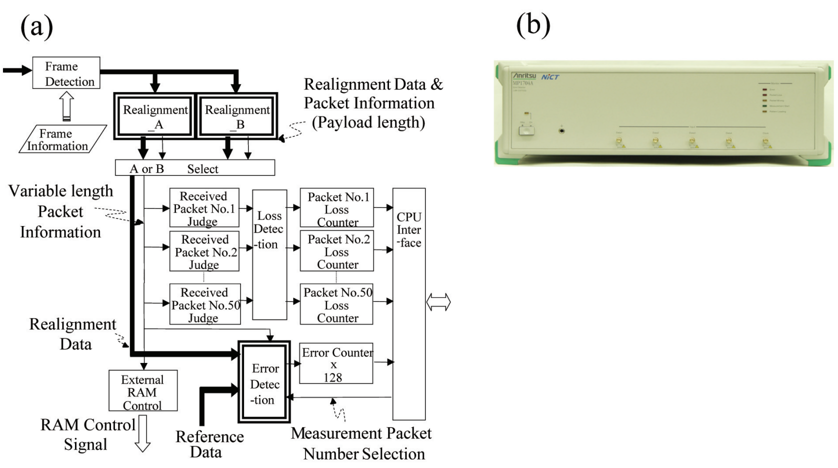

Fig.3 *FPGA architecture and external view of real-time BER & loss evaluation unit for 40-Gbit/s packet*

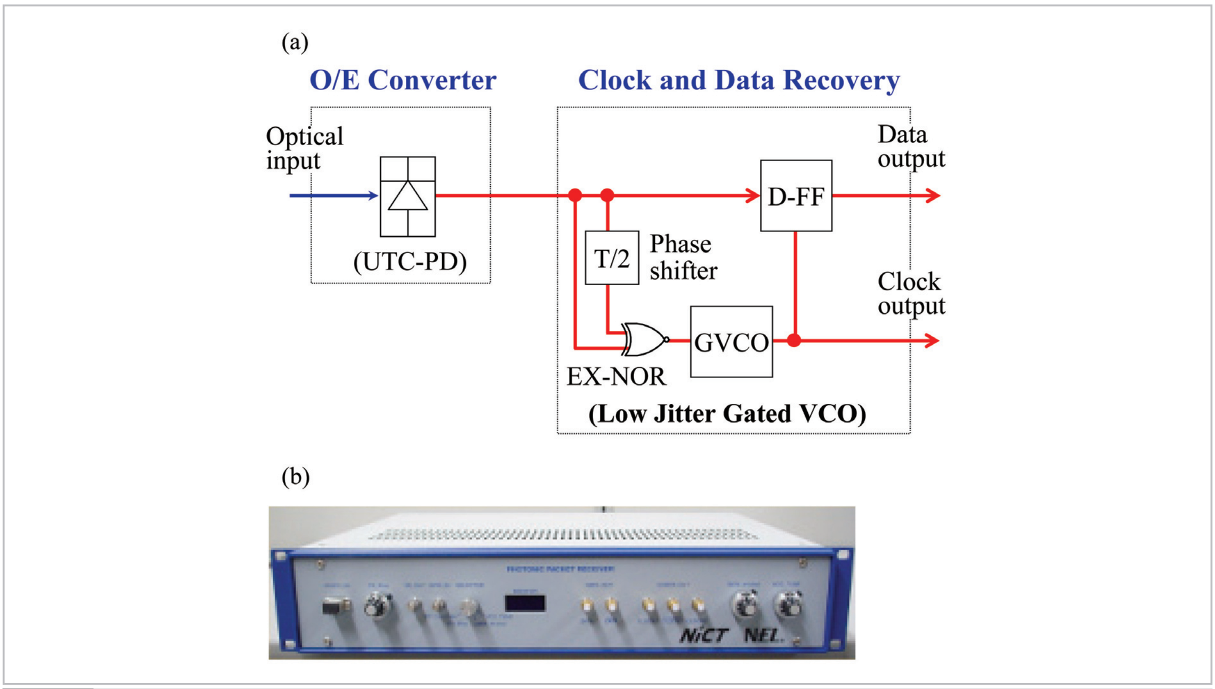

Fig.4 Architecture and external view of 10-Gbit/s packet receiver prototype

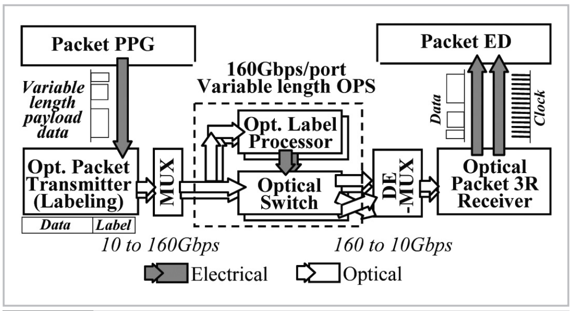

Fig.5 160-Gbit/s/port variable-length OPS experimental system

As shown in Fig.6, packet label analysis is performed based on parallel optical correlation in the time domain using OC. A single set of optical correlators functions as a label bank and records to the routing table the label corresponding to the destination node. When the codes match, the optical correlator outputs a high-intensity autocorrelation (AC) signal, and when they do not, it outputs a low-intensity cross-correlation (XC) signal. The payload is diffused in the time domain. As a result, label recognition may be carried out by setting a threshold signal intensity. However, when the payload bit rate (160 Gbit/s) is extremely close to the OC chip rate, the spectral band of the payload will nearly overlap with that of the OC (see Fig.7). In such a case, the intensity of the payload data diffused in the time domain may become larger than the XC signal intensity, thus allowing only a small margin up to the threshold value. To improve the intensity ratio between the AC signal and the diffused payload, an OC with a narrower spectral band was selected for our system[6]. Since the central wavelength of the OC pulse may be shifted from that of the payload pulse within the wavelength channel of interest, it is possible to achieve a high degree of discrimination in threshold processing by removing the diffused payload data components, using matched filtering and spectral filtering in correlation processing and extracting only the OC component.

Figure 8(a) shows a 160-Gbit/s variable-length packet having different labels, “A” and “B”, and Fig.8(b) shows the generated packet header, consisting of the optical label (L), preamble (P), frame pattern (F), sequence information (S: reference pattern, packet number, and pattern length), and payload data (D). Figure 8(c) is an eye-pattern diagram of the 160-Gbit/s payload data measured using an optical sampling oscilloscope.

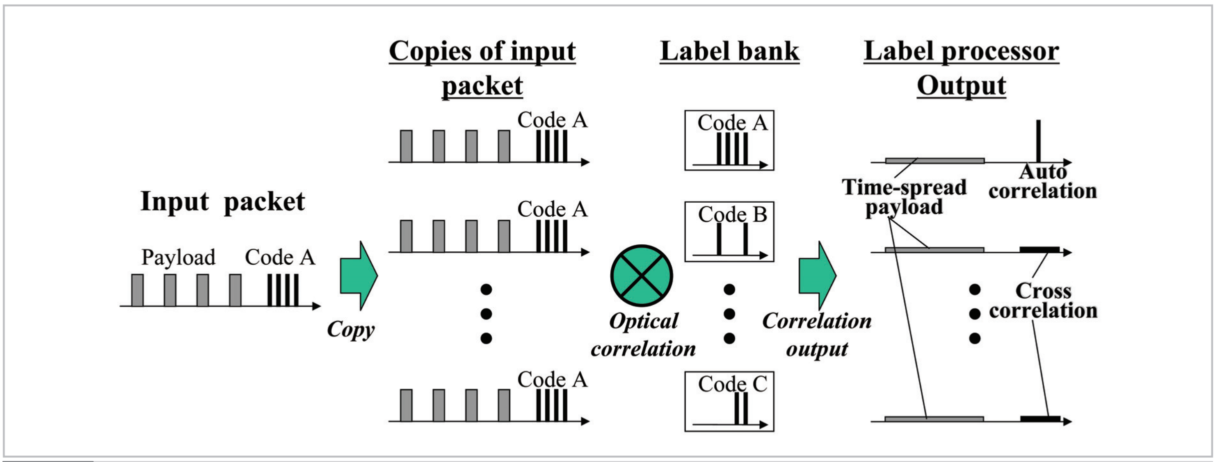

Fig.6 *Principle of all-optical parallel label processing*

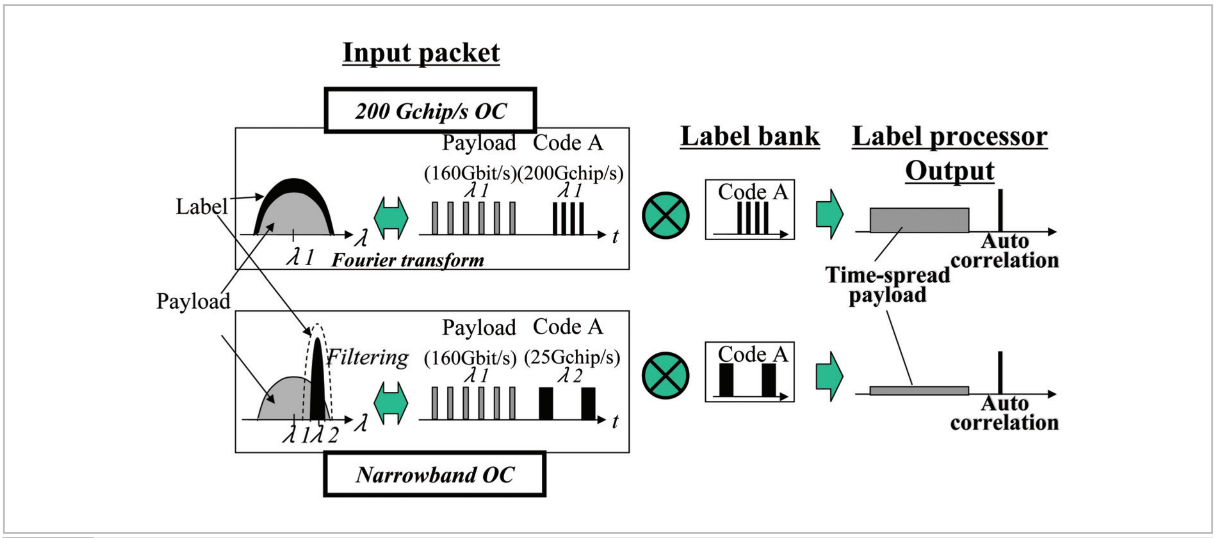

Fig.7 *Principle of narrow-band optical label processing*

Figure 8 (d) shows the spectra of the 160-Gbit/s data and the narrow-band (25 Gbit/s) BPSK optical label, and Fig.8(e) shows the 160-Gbit/s optical packet input to the optical switch (top), as well as the packet output from the switch (bottom). The results show fairly good performance for the 160-Gbit/s/port variable-length OPS. Figure 8(f) shows examples of output from the optical label processor for the cases of matched and non-matched labels (top), and the generated gate signals for switch control (bottom). Figure 8(g) shows the spectrum during DEMUX by four-wave mixing using highly nonlinear fibers and the demuxed 10-Gbit/s payload data. Figure 8(h) presents the clock reproduced by the optical packet 3R receiver and the eye-pattern for the data, together with the RF spectrum of the reproduced clock.

Figures 9(a) and (b) show the measured packet BER and loss, respectively. These results verify the performance of the ultra-high-speed variable-length OPS and its system to evaluate real-time characteristics.

4 The 160-Gbit/s/port OPS prototype

Figures 10 (a) and (b) show the architecture and an external view of the 160-Gbit/s/port OPS prototype, respectively. In narrow-band label processing, the optimal packet output port is determined by label analysis. The label processor controls the opti-

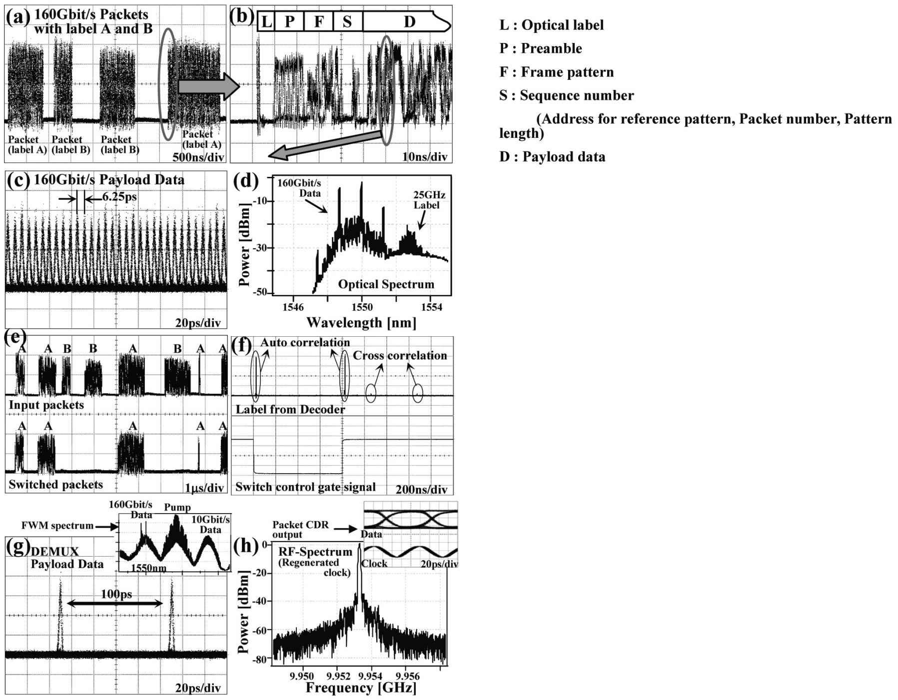

Fig.8 Results of 160-Gbit/s/port variable-length OPS experiment (1)

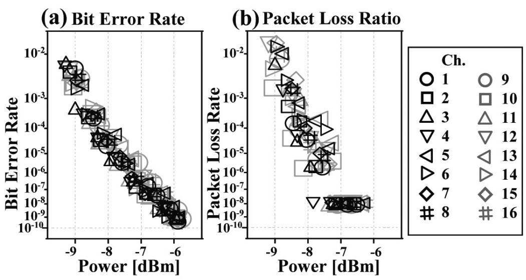

Fig.9 Results of 160-Gbit/s/port variable-length OPS experiment (2)

cal switch and relays the packet arrival information to the electronic scheduler. The scheduler controls the optical buffer and carries out contention resolution for the packets. The optical buffer stores the packets only for the necessary amount of time. At the optical buffer, the optical packets are switched to optical fiber delay lines (FDLs) of different lengths, where these switched packets are stored only for the necessary amount of time before they are re-merged and output from the output port. However, during this process, a reduction in the S/N ratio of the merged packet occurs due to the insufficient extinction ratio of the optical switches used in the buffer, interference between the switched packets, and the residual noise component. To overcome this problem, additional gate switches were introduced to remove the residual noise component in each FDL of the optical buffer.

In order to simplify the buffer architecture in the experiment, the packets were assumed to have fixed lengths. The duration of a single packet was 512 ns. The insertion losses of all components were corrected using an optical amplifier. A 10-GHz mode-locked laser diode (MLLD) with a central wavelength of 1,550.0 nm and a pulse width of 1.9 ps was used as the source for payload data generation at the transmitter. In order to use the narrow-band OC, the pulse width of the code-generation source was set at 4.0 ps at 1,552.8 nm. After reducing the pulse repetition period with the $LiNbO_3$ intensity modulator 1 (LN-IM1) to equal the packet generation period, 16-chip BPSK labels A and B, both featuring a chip rate of 25 Gchips/s, were generated by planar-lightwave-circuit (PLC) encoders 1 and 2, respectively. At the MUX for OTDM from 10

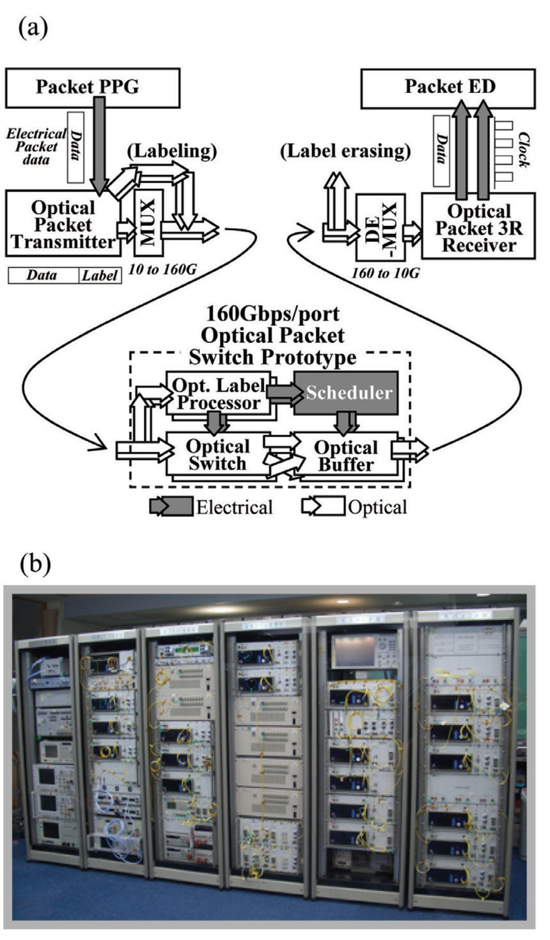

Fig.10 Block diagram and external view of a comprehensive test system using OPS prototype with 160-Gbit/s/port I/O interface

Gbit/s to 160 Gbit/s, the 10-Gbit/s payload generated by LN-IM2 was multiplexed to a 61, 440-bit 160-Gbit/s payload. Identical labels were appended to the beginning (as a label to open the optical switch) and to the end (as a label for closing the optical switch) of the payload. Then, the optical packets with labels A and B were replicated to create an input optical packet train to be sent to multiple input ports of the OPS prototype [see Fig.10 and Fig.11(a)].

In label processing, the payload data component is removed by matched filtering and spectral filtering, and matched filtering is performed on the label component. In our experiment, label processors 1 and 2 were employed to recognize only label A. Figure 11(b) shows the AC signal (for matched code), XC signal (for non-matched code), and the payload diffused in the time domain at processor 1. It can be seen that label A is correctly recognized and that the diffused payload is sufficiently suppressed. Next, electrical signals were output from the gate signal generator (GSG) to allow for opening/closing control of the optical switch, which consisted of a 1×2 optical coupler and a $LiNbO_3$ gate switch. Figure 11(c) illustrates the manner in which the switch opens and closes for an optical packet with label A.

The optical buffer consists of a 1×2 $LiNbO_3$ switch (LN-SW) and multiple FDLs of different lengths. The buffer size (maximum delay) is two packets (1,024 ns). In the present experiment, two LN-SWs were positioned for each FDL. The second switch is used for removing the residual noise component and achieving a high extinction ratio. The effectiveness of residual noise suppression by the buffer's dual-switch design is illustrated in Fig.11(d). Contention resolution is performed for the packets by relaying the control signal to the LN-SWs of buffers 1 and 2[4]. The FPGA-based electronic scheduler receives information on packet arrival timing from the label processor and begins the computation for scheduling. The buffered packets are then re-merged. Figures 11(e) and (f) show the buffered and re-merged optical packets, respectively. At the receiver, the 160-Gbit/s payload is demuxed to 10-Gbit/s with the OTDM-DEMUX system by FWM using highly nonlinear fibers. BER and the packet loss of the 10-Gbit/s payload are then measured with the evaluation system, which consists of a combination of the optical packet 3R receiver and the real-time packet BER measurement unit. The packet receivers perform real-time measurement of the random packet stream. Figure 11(g) shows the input packet data to the packet 3R receiver and the reproduced clock signal, and demonstrates the successful stable reproduction of the clocks from the randomly arriving burst streams of packet data. Figure 11(h) presents an eye-pattern of the received 10-Gbit/s payload data, and Fig.11(i)

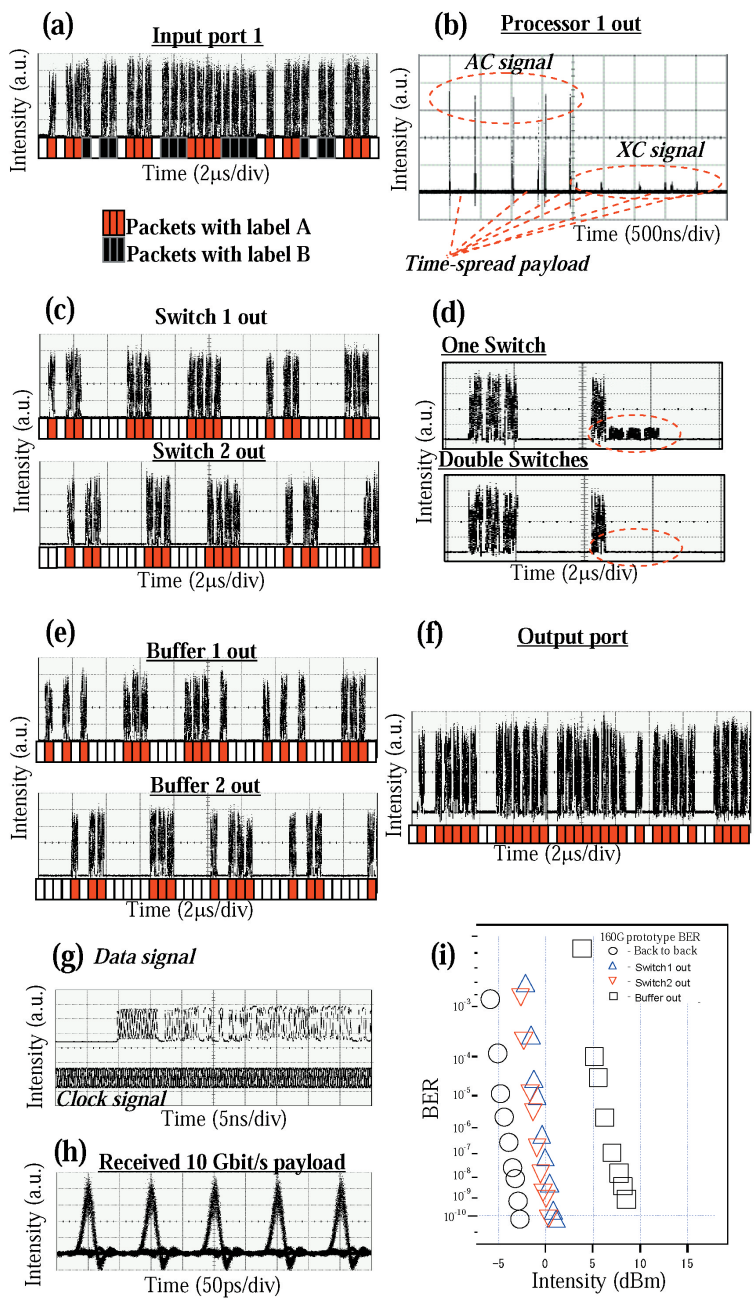

Fig. 11 *Results of experiment using OPS prototype with 160-Gbit/s/port I/O interface*

is the BER measured for the transmitting side, immediately after switching and buffering. The eye-pattern is clearly open, and the measured BER is below 10^{-10}. We can conclude from these results that the performance of ultra-high-speed optical packet switching has been successfully verified.

5 Conclusions

We have proposed a novel evaluation system for 40-Gbit/s variable-length packets, capable of real-time measurement of BER and packet loss for variable-length asynchronous-arrival random packets. A subsequent validation experiment was conducted on the generation and switching of 160 Gbit/s OTDM variable-length random packets by narrow-band OC label processing, and additionally, a combination evaluation system and an OTDM-DEMUX system was used to carry out a validation experiment on real-time measurement of BER and loss in variable-length packets. A 160 Gbit/s/port OPS prototype with functions for optical label processing, optical switching, optical buffering, electronic scheduling, optical MUX/DEMUX, and real-time measurement of packet BER and loss was produced and used in a comprehensive validation experiment of the ultra-high-speed OPS system, in order to confirm the effectiveness and stable operation of the present method.

It is of great significance to develop prototypes of these advanced photonic network technologies and to conduct more complete validation experiments using these technologies--i.e., to extend experimentation beyond bench-top demonstrations in the laboratory. Such prototype validation experiments will allow us to confirm the effectiveness of advanced technologies as well as to isolate the problems and themes applicable to the entire system at an early stage, and will also accelerate the construction of an actual photonic network.

Further, the real-time BER and packet loss measurement system for 40-Gbit/s variable-length packets and the optical packet 3R receivers, which were developed in the course of the present R&D effort (with the cooperation of the Anritsu Corporation and the NTT Electronics Corporation, respectively) are already being marketed by their respective companies, and it is our hope that these marketing efforts will contribute to the early realization of a photonic network.

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***WADA Naoya**, Ph.D.*

Reseaerch Manager, Ultrafast Photonic Network Group, New Generation Network Research Center (former: Senior Researcher, Ultrafast Photonic Network Group, Information and Network Systems Department)

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