16th IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC-2023)

Singapore University of Technology and Design, Singapore
December 18-21, 2023

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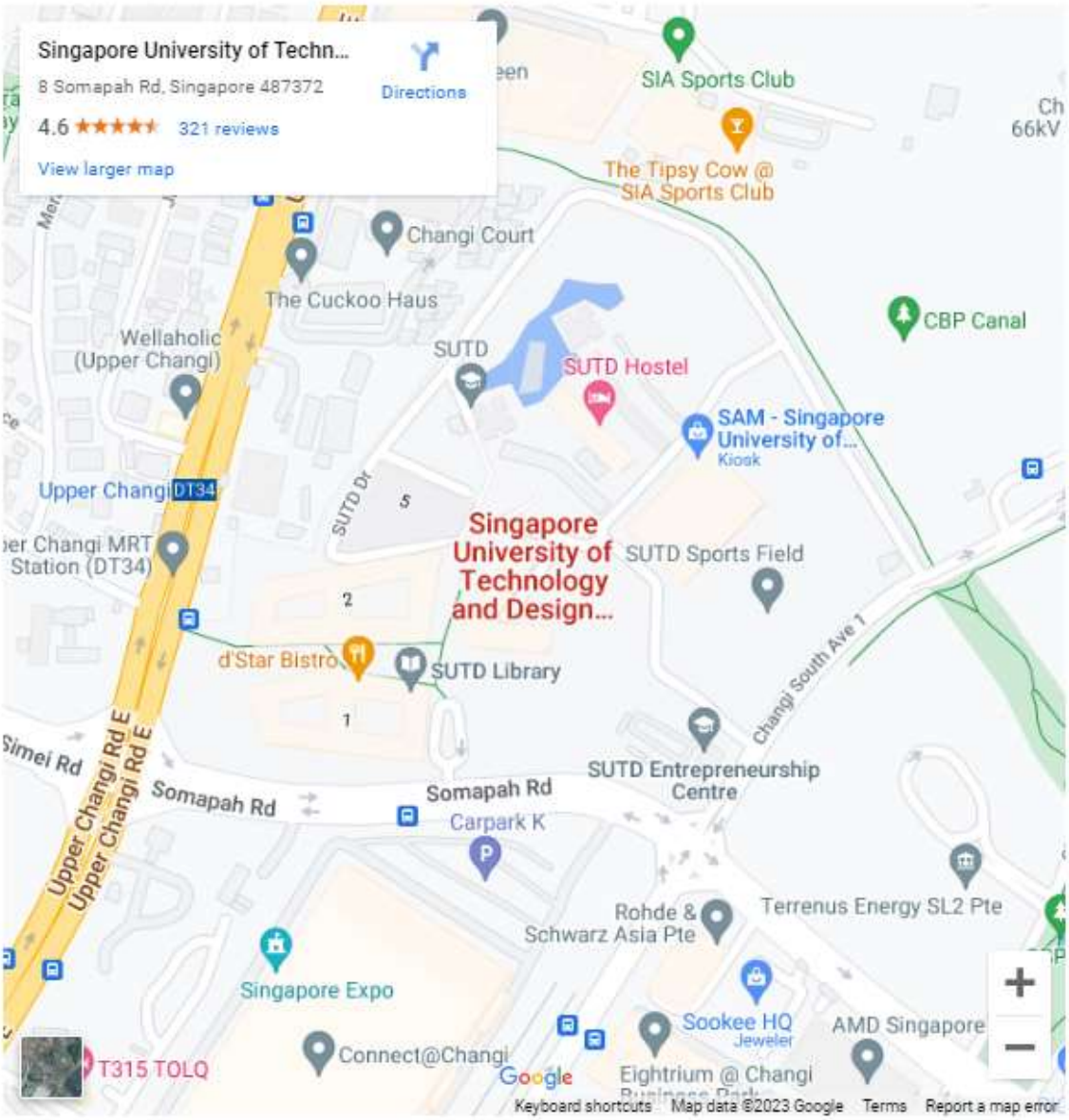

PROGRAM AT A GLANCE

Time	Room A	Room B
Monday, December 18, 2023		
14:00-14:05	O1: Kick-off Opening Session	
14:20-15:20	**A0: Multicore/Manycore SoCs Architecture.** Chair: Van-Phuc Hoang (Le Quy Don Technical University, Vietnam), Co-chair: Dang Nam Khanh (University of Aizu, Japan)	**B0: Multicore/Manycore SoCs Architectures & Applications.** Chair: Omar Hammami (ENSTA PARIS, France), Co-chair: Yoshiki Yamaguchi (University of Tsukuba, Japan)
15:30-16:30	**A1: Low-power Solutions for Future SoC Design**. Chair: Hayate Okuhara (National University of Singapore, Singapore), Co-chair: Yuan He (Keio University, Japan)	**B1: Distributed Computing and Communication Techniques for Emerging AI Applications.** Chair: Zixia Shang (University of New South Wales, China), Co-chair: Chinmay Dhawan (Thoughtworks Technologies, India)
16:40-17:40	**A2: Embedded Applications and Ubiquitous Computing**. Chair: Yuan He (Keio University, Japan), Co-chair: Akram Ben Ahmed (National Institute of Advanced Industrial Science and Technology (AIST), Japan)	**B2: Embedded, Cyber-Physical, and IoT Systems.** Chair: Tran Hoa (Kumoh National Institute of Technology, South Korea), Co-chair: Williams Yerima (University of Aizu, Japan)
Tuesday, December 19, 2023		
09:00-09:20	O2: Opening Session	
09:20-10:20	Keynote 01:Takahiro Hanyu, Professor, Tohoku University, Japan. Title: "**Challenge of MTJ-Based Nonvolatile Hardware for Edge AI Applications**" Chair: Yuan He (Keio University, Japan)	
10:30-11:30	A3: **Multicore/Manycore SoCs Applications & Designs – I**. Chair: Hiroshi Saito (The University of Aizu, Japan), Co-Chair: Shaswot Shresthamali (Keio University, Japan)	**B3: Emerging Machine Learning and Deep Learning Models: Theory and Applications – I**. Chair: Wonjik Kim (National Institute of Advanced Industrial Science and Technology, Japan), Co-chair: MD. Al Mehedi Hasan (Rajshahi University of Engineering & Technology, Bangladesh)
13:30-14:30	Keynote 2: Khein-Seng Pua, Founder and CEO of Phison Electronics, Taiwan. Title: "**Challenges and Opportunities of Next-Generation Enterprise SSD Storage**." Chair: Lan-Da Van (National Yang Ming Chiao Tung University, Taiwan), Co-chair: Yue Zheng (Chinese University of Hong Kong, Shenzhen, China).	
14:40-15:40	**A4: Multicore/Manycore SoCs Programming & Architecture – I**. Chair: Josna VR (Cochin Univ. of Science . and Technology, India), Co-chair: Ruchika Gupta (Chandigarh University, India),	**B4: Emerging Machine Learning and Deep Learning Models: Theory and Applications – II.** Chair: Yoichi Tomioka (University of Aizu, Japan), Co-chair: Yue Zheng (The Chinese University of Hong Kong, Shenzhen, China)
15:50-16:50	A5: **Multicore/Manycore SoCs Programming & Architecture – II.** Chair**:** John Jose (Indian Institute of Technology Guwahati, India), Co-chair: Meisam Abdollahi (University of Victoria, Canada)	**B5: Parallel/Distributed, Grid, and Cloud Computing.** Chair: Zhishang Wang (University of Aizu, Japan), Co-chair: Huakun Huang (Guangzhou University, China)
17:00-18:00	**A6:Multicore/Manycore SoCs Programming and Architecture – III** Chair: Kun-Chih Chen (National Yang Ming Chiao Tung University, Taiwan), Co-chair: John Jose (Indian Institute of Technology Guwahati, India)	**B6:Emerging Machine Learning and Deep Learning Models: Theory and Applications – III** Chair: Wonjik Kim (National Institute of Advanced Industrial Science and Technology, Japan), Co-chairs: Incheon Paik, (University of Aizu, Japan), Qinglin Yang (Sun Yat-Sen University, China)
Wednesday, December 20, 2023		

09:00-10:00	K3:Mahdi Nikdast, Associate Professor, Colorado State University, USA. Title: "**The Silicon Photonics Marathon: From Optical Interconnect to Computing and Memory!**" Chair: Michael Meyer (Eastern Washington University, USA)	
10:10-11:10	**A7: Machine Learning and Neuromorphic Computing for Edge and IoT.** Chair: Michael Meyer (Eastern Washington University, USA), Co-chair: Yasser Ismail (Southern University and A&M College, USA)	**B7: Multicore/Manycore SoCs Programming & Architecture – IV.** Chair: Trong-Thuc Hoang (University of Electro-Communications (UEC), Tokyo, Japan)
14:00-14:55	Tutorial 1: "**E-Textile Pressure Sensors and Their Applications"**. Prof. Lei Jing (The University of Aizu, Japan)	
15:10-16:10	**A8: Multicore/Manycore SoCs Applications & Designs – II** Chair: Michael Meyer (Eastern Washington University, USA), Tanja Harbaum (Karlsruhe Institute of Technology (KIT), Germany)	**B8:Neuromorphic Computing Systems & AI on Edge.** Chairs: Khanh N. Dang (University of Aizu, Japan), Daisuke Suzuki (The University of Aizu, Japan)
16:20-17:20	**A9: Multicore/Manycore SoCs Programming & Architecture – V** Chair: Hiroki Nakahara (Tohoku University, Japan), Co-chair: Razaidi Hussin (Universiti Malaysia Perlis, Malaysia)	**B9: Emerging Machine Learning and Deep Learning Models: Theory and Applications – IV** Chair: Masato Motomura (Tokyo Institute of Technology, Japan), Co-Chair: Wonjik Kim (National Institute of Advanced Industrial Science and Technology, Japan)
Thursday, December 21, 2023		
09:00-10:00	Keynote 4: Steven Fong, Managing Director, AMD South Asia Pacific Sales, Singapore. Title: "**Accelerating Silicon technology to deliver the exponential growth in Compute"**	
10:10-11:10	**A10: Embedded Multicore/Manycore SoC Architectures and Programming.** Chair: Pham Hoai Luan (Nara Institute of Science and Technology, Japan), Co-chair: Kasem Khalil (University of Mississippi, USA)	**B10: Performance Optimization and Auto-Tuning of Software on Multicore/Manycore Systems** Chair: Kazuhiko Komatsu (Tohoku University, Japan)
11:50-12:00	Closing session	

Notes:

- Time and date are in the Singapore time zone (GMT+8).
- Time is in a 24-hour time format
- For the online program, please visit: https://mcsoc-forum.org/site/index.php/program/
- For online discussion on Slack: http://ieeemcsoc2023.slack.com/
- For any questions or inquiries, please feel free to contact us.

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MESSAGE FROM THE CHAIRS

Welcome to the 2023 IEEE 16th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (IEEE MCSoC-2023)

The 2023 IEEE 16th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC-2023) is an annual international symposium sponsored by IEEE, the Technical Committee on Microprocessors and Micro-computers of the IEEE Computer Society in cooperation with the IEEE Singapore Section. MCSoC 2023 is hosted in Singapore at the Singapore University of Technology and Design (SUTD).

There is growing confidence that future system-on-chips and high-performance systems will be based on connectionist models, and the innovative design of interconnection networks, processor architecture, applications, and software tools for embedded multi-core systems-on-chip will play a crucial role in our understanding of future systems. Along with Industry 4.0, the Internet of Things, cloud computing, data-centric computing through the Internet, and artificial intelligence become more and more popular. Therefore, the required computing power is incredibly increasing every moment.

The rise of artificial intelligence innovation in recent years is encountering efficiency of power, online adaptation, and architectural and design issues. This edition of MCSoC offers new tracks on artificial intelligence on-chip learning and neuromorphic computing together with nine tracks on SoC design and application to bring new and potent methods for design from devices to applications.

We hope the 16th edition of the IEEE MCSoC 2023 symposium will significantly contribute to these very challenging computer science and engineering fields. We want to thank all sponsors, authors, keynotes, and participants.

We hope you will find your participation rewarding and your stay in Singapore enjoyable.

16th IEEE MCSoC 2023 Chairs

K1: Keynote 1

Room: Room A

Monday, December 20, 2023. Time: 09:20- 10:20 (GMT+8)

Title*:* Challenge of MTJ-Based Nonvolatile Hardware for Edge AI Applications

Takahiro Hanyu, Professor, Tohoku University, Japan

Biography: Takahiro Hanyu received the B.E., M.E., and D.E. degrees in Electronic Engineering from Tohoku University, Sendai, Japan, in 1984, 1986, and 1989, respectively. He is currently a full professor and the director (from April 2022 to present) at the Research Institute of Electrical Communication, Tohoku University. His general research interests include nonvolatile logic circuits, their applications to ultra-low-power and/or highly dependable VLSI processors and post-binary computing, and their application to brain-inspired VLSI systems and edge AI hardware. He received the Sakai Memorial Award from the Information Processing Society of Japan in 2000, the Judge's Special Award at the 9th LSI Design of the Year from the Semiconductor Industry News of Japan in 2002, the Special Feature Award at the University LSI Design Contest from ASP-DAC in 2007, the APEX Paper Award of Japan Society of Applied Physics in 2009, the Excellent Paper Award of IEICE, Japan, in 2010, the Ichimura Academic Award in 2010, the Best Paper Award of IEEE ISVLSI 2010, the Paper Award of SSDM 2012, the Best Paper Finalist of IEEE ASYNC 2014, and the Commendation for Science and Technology by MEXT, Japan, in 2015. Dr. Hanyu is a Senior Member of the IEEE.

Abstract: Nonvolatile spintronic devices have potential advantages such as fast read/write and high endurance together with back-end-of-the-line compatibility of semiconductor fabrication, which offers the possibility of constructing not only stand-alone RAMs and embedded RAMs that can be used in conventional VLSI circuits and systems but also realizing standby-power-free and high-performance VLSI processors, which could open up a practical intermittent-computing paradigm for internet-of-things (IoT) applications. My presentation presents some AI-hardware examples based on MTJ-based nonvolatile logic-in-memory architecture, and their suitability for IoT applications is discussed

K2: Keynote 2

Room: Room A

Tuesday, December 19, 2023. Time: 13:20 – 14:30 (GMT+8)

Title: Challenges and Opportunities of Next-Generation Enterprise SSD Storage

Khein-Seng Pua, Founder and CEO of Phison Electronics, Taiwan

Biography: KS Pua is the Founder and CEO of Phison Electronics. He was born in a farming community Sekinchan in Selangor, Malaysia, in 1974. At the age of 19, he went to Taiwan with just US$4,000 in his pocket. With no relatives to help him, his only dream was to study hard; he graduated from National Chiao Tung University (NCTU) in Hsinchu, Taiwan, in 1997 and earned a Master's from NCTU in 1999. Mr. Pua and his four friends founded Phison Electronics Corp. in Taiwan. He designed and produced the world's first single-chip USB flash controller with other founders. Under his leadership, the company has become a global leader in NAND Flash controller IC and storage solutions. As an entrepreneur, Mr. Pua is a successful high-tech entrepreneur and the recipient of the Ten Outstanding Young Malaysian Awards and received the Outstanding Young Entrepreneur Award, the Outstanding Young Manager Award, and The President Award of National Management Excellence Award from the Government. He was elected a Fellow of the Chinese Society for Management Of Technology in 2009. In 2020, Phison enjoyed a turnover of US$1.64 billion and became the largest independent NAND controller and NAND storage solution provider globally, and was named 65th in U.S magazine Bloomberg Businessweek's Tech 100 in the year of 2010. From 2015 to the present, the production value of Phison was ranked top 4 IC Design Houses in Taiwan's IC design industry.

Abstract: Data is driving the transformation of the world, including the Internet of Everything, AI, and high-speed computing technologies. All of these are driving the digital transformation of all industries and assisting humans and enterprises to make faster and more accurate decisions through data analysis and artificial intelligence. In such a transformation process, data storage and reading and writing behaviors play a very important role; for example, the computing results of artificial intelligence come from the collection of big data, the foundation of cloud services comes from the construction of data centers, and the server environment for high-speed computing comes from the matching stable and high-speed enterprise-level storage architecture. What kind of challenges and opportunities will enterprise SSDs face due to the transformation of these digital technologies? Welcome to the keynote speech of KSPua, CEO of Phison, to explore the latest enterprise SSD technologies and development trends.

K3: Keynote 3

Room: Room A

Wednesday, December 20, 2023. Time: 09:00-10:00 (GMT+8)

Title: The Silicon Photonics Marathon: From Optical Interconnect to Computing and Memory!

Mahdi Nikdast, Associate Professor, Colorado State University, USA

Biography: Mahdi Nikdast is an Associate Professor and Endowed Rockwell-Anderson Professor in the Department of Electrical and Computer Engineering at Colorado State University (CSU), Fort Collins, where he is directing the Electronic-PhotoniC System Design (ECSyD) Laboratory. He received his Ph.D. in Electronic and Computer Engineering from The Hong Kong University of Science and Technology (HKUST), Hong Kong, in 2014. From 2014 to 2017, he was a postdoctoral fellow at McGill University and Polytechnique Montreal, Quebec, Canada. His research interests are at the intersection of integrated photonics, emerging technologies, and high-performance computing. Prof. Nikdast and his students have published numerous papers in refereed journals and international conference publications and across different areas of VLSI, EDA, Photonics, Embedded Systems, Systems-on-Chip (SoCs), Artificial Intelligence (AI), and Computer Architecture. He has edited a book on Silicon Photonics for High-Performance Computing and Beyond, published by Taylor and Francis Group in 2022, and another book on Photonic Interconnects for Computing Systems: Understanding and Pushing Design Challenges, published by River Publishers in 2017. Prof. Nikdast currently serves as an Associate Editor for IEEE Transactions on Very Large Scale Integration Systems (IEEE TVLSI), and has served on the TPC of various international conferences, including DAC, OFC, DATE, ICCAD, ESWEEK, NOCS, etc. He is a co-founder of the International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS workshop) and the North American Workshop on Silicon Photonics for High-Performance Computing (SPHPC Workshop). Prof. Nikdast and his team were the recipient of various awards, including the Second Best Project Award at the AMD Technical Forum and Exhibition (AMD-TFE 2010, Taiwan), the Best Paper Award at the Asia Communications and Photonics Conference (ACP 2015, Hong Kong), the Best Paper Award at the Design, Automation, and Test in Europe (DATE) Conference (DATE 2016 – Test Track, Dresden), the Best Paper Award Candidate at ACM Great Lake Symposium on VLSI (GLSVLSI 2018, USA), and the Best Paper Honorable Mention Award at ACM Great Lake Symposium on VLSI (GLSVLSI 2020, China). Prof. Nikdast received the prestigious NSF CAREER Award (2021), the George T. Abell Award for Outstanding Early-Career Faculty (2022), the Rockwell-Anderson Professorship (2022), and the George T. Abell Award for Teaching and Mentoring (2023). He is a Senior Member of the IEEE.

Abstract: Silicon photonics technology has facilitated the deployment of integrated photonics across different application domains, from ultra-fast communication for chip-scale interconnect and Datacom applications to energy-efficient optical computation for accelerating AI and machine learning applications. More recently, the integration of silicon photonics and nonvolatile phase change materials has also created a unique opportunity to realize photonic memory and in-memory optical computing. In this keynote, through an interdisciplinary approach and from device to system level, I will present a holistic overview of the promise and challenges of silicon photonics when employed for inter- and intra-chip optical interconnect AI acceleration and memory applications. I will present several examples of many-core systems-on-chip (SoCs) integrating silicon photonics and how to design solutions based on hardware-software co-design and cross-layer co-optimization that can efficiently address some of the existing challenges in such systems.

K4: Keynote 4

Room: Room A

Thursday, December 21, 2023. Time: 09:00- 10:00 (GMT+ 8)

Title: Accelerating Silicon technology to deliver the exponential growth in Compute

Steven Fong, Managing Director, AMD South Asia Pacific Sales, Singapore

Biography: Steven Fong has been Managing Director for AMD South Asia Pacific Sales since the merger of AMD/Xilinx. Prior**,** he spent 11 years (2008-2022) with Xilinx across multiple roles as Senior Director. Steven had established the Global Pricing group and was managing both Xilinx's worldwide strategic and field tactical pricing. Several world-class business models are now intrinsic to AMD Adaptive Embedded Computing Group's commercial principles. The newly built pricing establishment has become an essential cornerstone to enable Xilinx's world-class growing Gross margin from 2009 (GM 64%) to 2019 (GM 73%). Steven also doubled his role to establish Xilinx's worldwide first consumer strategy (2014~2016) and is a sitting member of AMD Singapore leadership council till now. Steven founded Xilinx South Asia Pacific Sales Group (2019) and doubled the business over three years. Before Xilinx, Steven spent 13 years in STMicroelectronics as a regional & and global marketing/business leader for Analog products. He established STMicroelectronic's first Asian-based Global strategic business unit in 2004 and doubled the revenue/margin over four years. Steven graduated with an honor degree (Electronic Engineering, 1995) from Nanyang Technological University. He also has a Master in Management (2006) from the Macquarie Graduate School of Management, an MBA (2008) from the University of Western Australia, and a Postgraduate Diploma from the Chartered Institute of Marketing (UK).

Abstract: As we migrate up the use case on vast data collected globally over decades, the need for computing grows to manage that transition. There is a huge implication for the accelerated push on silicon technology to deliver that compute level. With Moore's law diminishing after decades of keeping up the double in 2 years, this poses an exponential challenge to deliver the desired compute in a silicon device. The industry needs to innovate to compensate for the decelerating Moore law. One of the changes that allow us to keep up is Advanced packaging, which has grown in importance to the performance of the device. Using 2D, 2.5D, 3D with better TSV, interposer, and interconnect will soon become the next norm. Another emerging side effect of expanding computing is the need for power and thermal management. With the infinite number of connected devices over the next decades, the semiconductor industry has an impact on world energy. This raises the importance of performance per watt, especially from the recent impact of Generative AI on data centers.

Monday, December 18, 2023

Monday, December 18, 2023. Time: 14:00 – 14:05 (GMT+8)

O1: Kick-off Session

Room: Room-A

Monday, December 18, 2023. Time: 14:20 – 15:20 (GMT+8)

A0: Multicore/Manycore SoCs Architecture.
Chair: Van-Phuc Hoang (Le Quy Don Technical University, Vietnam), Co-chair: Dang Nam Khanh (University of Aizu, Japan)

Room: Room-A

14:20 ***Hybrid Hardware-Software Architecture for Quantum Secure IoT Embedded Systems***
Aobo Li, Jiahao Lu, Dongsheng Liu and Xiang Li (Huazhong University of Science and Technology, China); Shuo Yang (Huazhong University of Science and Technology & School of IC, China); Jiaming Zhang, Tianze Huang and Siqi Xiong (Huazhong University of Science and Technology, China)

14:35 ***Revealing Secret Key from Low Success Rate Deep Learning-Based Side Channel Attacks***
Van-Phuc Hoang and Ngoc-Tuan Do (Le Quy Don Technical University, Vietnam); Trong-Thuc Hoang (The University of Electro-Communications, Japan); Cong-Kha Pham (University of Electro-Communications (UEC), Japan)

14:50 ***Multi-objective Optimisation of RISC-V CV32A6 for ML application***
Omar Hammami (ENSTA Paris, France)

15:05 ***An open-source and GUI-capable RISC-V computer system on a low-end FPGA board***
Kenji Kise (Tokyo Institute of Technology, Japan)

Monday, December 18, 2023. Time: 14:20 – 15:20 (GMT+8)

B0: Multicore/Manycore SoCs Architectures & Applications.
Chair: Omar Hammami (ENSTA PARIS, France), Co-chair: Yoshiki Yamaguchi (University of Tsukuba, Japan)

Room: Room-B

14:20 ***A remote partial-reconfigurable SoC with a RISC-V soft processor targeting low-end FPGAs***
Yuji Yamada, Nesrine Berjab, Tomohiro Yoneda and Kenji Kise (Tokyo Institute of Technology, Japan)

14:35 ***Reinforcement Learning Enabled Multi-Layered NoC for Mixed-Criticality Systems***
Nidhi Anantharajaiah, Fabian Lesniak, Tanja Harbaum and Juergen Becker (Karlsruhe Institute of Technology, Germany)

14:50 ***An Energy-Efficient Re-configurable Multi-Mode Convolution Neuron Network Accelerator***
T. Hui Teo (Singapore University of Technology and Design, Singapore); I-Chyn Wey (Chang Gung University, Taiwan); Huan-Ke Hsu (Singapore University of Technology and Design, Singapore)

15:05 Free slot

Monday, December 18, 2023. Time: 15:30 – 16:30 (GMT+8)

A1: Low-power Solutions for Future SoC Design.
Chair: Hayate Okuhara (National University of Singapore, Singapore), Co-chair: Yuan He (Keio University, Japan)

Room: Room-A

15:30 ***A cost/power efficient storage system with directly connected FPGA and SATA disks***
Ryohei Niwase and Hkaru Harasawa (University of Tsukuba, Japan); Yoshiki Yamaguchi (University of Tsukuba, Japan & Kumamoto University, Japan); Kaijie Wei and Hideharu Amano (Keio University, Japan)

15:45 ***An Area-Efficient Coarse-Grained Reconfigurable Array Design for Approximate Computing***
Kaito Kutsuna, Takuya Kojima, Hideki Takase and Hiroshi Nakamura (The University of Tokyo, Japan)

16:00 ***Design of The Ultra-Low-Power Driven VMM Configurations for uW Scale IoT Devices***
Keisuke Takano, Takeaki Yajima and Satoshi Kawakami (Kyushu University, Japan)

16:15 ***LCT-TL: Learning Classifier Table (LCT) with Transfer Learning for run-time SoC performance-power optimization***
Anmol Surhonne, Florian Maurer, Thomas Wild, and Andreas Herkersdorf (Technical University of Munich, Germany)

Monday, December 18, 2023. Time: 15:30 – 16:30 (GMT+8)

B1: Distributed Computing and Communication Techniques for Emerging AI Applications.
Chair: Zixia Shang (University of New South Wales, China), Co-chair: Chinmay Dhawan (Thoughtworks Technologies, India)

Room: Room-B

15:30 ***Overcoming Limited Data Challenges: Training Large-Scale Deduplication Models through Distributed and Non-Distributed Methods***
Shraddha Surana, Chinmay Dhawan, Digvijay Gunjal and Rajesh Tamhane (Thoughtworks Technologies, India)

15:45 ***OCA – Code Advisory Tool for OpenMP Parallelization of Sequential Code***
Gadi Haber (Intel, IDC., Israel); Yosi Ben Asher (CS. University of Haifa, Israel); Shachaf Altman (Software Compilation, Israel); Cfir Aguston (Software, Israel)

16:00 ***Context-Aware Layer Scheduling for Seamless Neural Network Inference in Cloud-Edge Systems***
Matthias Stammler, Vladimir Sidorenko, Fabian Kreß, Patrick Schmidt and Juergen Becker (Karlsruhe Institute of Technology, Germany)

16:15 ***Patient Similarity Using Electronic Health Records and Self-supervised Learning***
Hong Dao Ngoc and Incheon Paik (The University of Aizu, Japan)

Monday, December 18, 2023. Time: 16:40 – 17:40 (GMT+8)

A2: Embedded Applications and Ubiquitous Computing.
Chair: Yuan He (Keio University, Japan), Co-chair: Akram Ben Ahmed (National Institute of Advanced Industrial Science and Technology (AIST), Japan)

Room: Room-A

16:40 ***Integrated 3D Active Noise Cancellation Simulation and Synthesis Platform Using Tcl***
Seunghyun Park (Kyungpook National University, Korea (South)); Daejin Park (Kyungpook National University (KNU), Korea (South))

16:55 ***Enhancing Road Safety with Cloud-Integrated IoT Road Signal Detection System***
Antoine Hitayezu and Umutoni M Ritha (University of Rwanda, Rwanda); Emmanuel Tuyishime (Transilvania University of Brasov, Romania); Kayalvizhi Jayavel (Kayalvizhi Jayavel, Creative Computing Institute, University of Arts, London, UK); Charles Kabir (University of Rwanda, Rwanda)

17:10 ***SwinGaze: Egocentric Gaze Estimation with Video Swin Transformer***
Xinghe Wang (Guilin University Of Electronic Technology, China); Yujie Li (Guilin University of Electronic Technology, China); Zihang Ma and Yifu Wang (Guilin University Of Electronic Technology, China); Michael C Meyer (Eastern Washington University, USA)

17:25 **Free slot**

Monday, December 18, 2023. Time: 16:40 – 17:40 (GMT+8)

B2: Embedded, Cyber-Physical, and IoT Systems.
Chair: Tran Hoa (Kumoh National Institute of Technology, South Korea), Co-chair: Williams Yerima (University of Aizu, Japan)

Room: Room-B

16:40 ***An Efficient Bandit Learning for Matching based Distributed Task Offloading in Fog Computing Network***
Tran Hoa and Dong Seong Kim (Kumoh National Institute of Technology, Korea (South))

16:55 ***IODnet: Indoor/Outdoor Telecommunication Signal Detection through Deep Neural Network***
Meisam Abdollahi (University of Victoria, Canada); Sepideh Mashhadi (Iran University of Science and Technology, Iran); Alireza Mirzaei, Ramin Sabzalizadeh and Mohammad Elahi (Mobile Telecommunication Company of Iran, Iran); Amir Baharloo and Amirali Baniasadi (University of Victoria, Canada)

17:10 ***A novel fire monitoring system for electric bicycle shed based on YOLOv8***
Hongyang Zhong, Ziwen Wang, Zhiyi Chen, Wenhao Chen and Yujie Li (Guilin University of Electronic Technology, China)

17:25 ***Analysis of the Influence of Instagram Social Media Use on User's Consumptive Behavior***
Kevin Fernando Edlanda, Stanley Kent Purnama, and Anderes Gui (Bina Nusantara University, Indonesia); Anwar Allah Pitchay (Universiti Sains Malaysia, Malaysia)

****End of Day 1****

Tuesday, December 19, 2023

Tuesday, December 19, 2023. Time: 9:00 – 9:20 (GMT+8)

O2: Opening Session

Room: Room-A

Tuesday, December 19, 2023. Time: 9:20 – 10:20 (GMT+8)

Keynote 01:Takahiro Hanyu, Professor, Tohoku University, Japan. Title: ”Challenge of MTJ-Based Nonvolatile Hardware for Edge AI Applications”

Chairs: Yuan He (Keio University, Japan)
Room: Room-A

Tuesday, December 19, 2023. Time: 10:30 – 11:30 (GMT+8)

A3: Multicore/Manycore SoCs Applications & Designs – I.
Chair: Hiroshi Saito (The University of Aizu, Japan), Co-Chair: Shaswot Shresthamali (Keio University, Japan)

Room: Room-A

10:30 ***A Convolutional Neural Network Inference Accelerator Design using Algorithmic Noise-Tolerance Technology***
T. Hui Teo and Shih-Yi Yang (Singapore University of Technology and Design, Singapore); I-Chyn Wey (Chang Gung University, Taiwan); Huan-Ke Hsu (Singapore University of Technology and Design, Singapore)

10:45 ***Evaluation Model for Current-Domain SRAM-based Computing-in-Memory Circuits***
Yiran Zhang, Bo Wang, Jinwu Chen, Xi Chen, Xin Si (Southeast University, China)

11:00 ***Convolution Neural Networks Inference Accelerator Design using Selective Convolutional Layer***
T. Hui Teo, Tzu-Huan Huang, and Emil Goh (Singapore University of Technology and Design, Singapore); I-Chyn Wey (Chang Gung University, Taiwan)

11:15 ***Efficient Resource-Aware Neural Architecture Search with a Neuro-Symbolic Approach***
Davide Bertozzi (University of Manchester, United Kingdom (Great Britain)); Elena Bellodi, Alice Bizzarri, Michele Favalli, Michele Fraccaroli and Riccardo Zese (University of Ferrara, Italy)

Tuesday, December 19, 2023. Time: 10:30 – 11:30 (GMT+8)

B3: Emerging Machine Learning and Deep Learning Models: Theory & Applications – I.
Chair: Wonjik Kim (National Institute of Advanced Industrial Science and Technology, Japan), Co-chair: MD. Al Mehedi Hasan (Rajshahi University of Engineering & Technology, Bangladesh)

Room: Room-B

10:30 ***Combining Decision Tree and Convolutional Neural Network for Energy-Efficient On-Device Activity Recognition***
Marius Brehler and Lucas Camphausen (Fraunhofer IML, Germany)

10:45 ***Reliability Estimation of ML for Image Perception: A Lightweight Nonlinear Transformation Approach Based on Full Reference Image Quality Metrics***
Joao Vitor Zacchi, Francesco Carella, Priyank Upadhya and Shanza Ali Zafar (Fraunhofer IKS, Germany); John Molloy (University of York, United Kingdom); Lisa Jöckel and Janek Groß (Fraunhofer IESE, Germany); Núria Mata and Nguyen Anh Vu Doan (Fraunhofer IKS, Germany)

11:00 ***Graph structure and homophily for label propagation in Graph Neural Networks***
Maxence Vandromme (France); Serge Petiton (Lille University of Science and Technology, France)

11:15 ***Iterative Refinement Quantum Amplitude Estimation***
Yoshiyuki Saito and Nobuyoshi Asai (University of Aizu, Japan); Jungpil Shin (University of AIZU, Japan); Dongsheng Cai, Xinwei Lee and Ningyi Xie (University of Tsukuba, Japan)

Tuesday, December 19, 2023. Time: 13:30 – 14:30 (GMT+8)

Keynote 2: Khein-Seng Pua, Founder and CEO of Phison Electronics, Taiwan. Title: ”Challenges and Opportunities of Next-Generation Enterprise SSD Storage”

Chair: Lan-Da Van (National Yang Ming Chiao Tung University, Taiwan), Co-chair: Yue Zheng (Chinese University of Hong Kong, Shenzhen, China).

Room: Room-A

Tuesday, December 19, 2023. Time: 14:40 – 15:40 (GMT+8)

A4: Multicore/Manycore SoCs Programming & Architecture – I.
Chair: Josna VR (Cochin Univ. of Sci. and Technology, India), Co-chair: Ruchika Gupta (Chandigarh University, India)

Room: Room-A

14:40 ***A performance prediction for automatic placement workloads on many-cores***
Stéphane Louise (CEA, LIST, France); Nicolas Benoit (Serviware, France)

14:55 ***Board Allocation Algorithm for the Resource Management System of FiC***
Takumi Inage, Kensuke Iizuka and Hideharu Amano (Keio University, Japan)

15:10 ***GRONA: A Framework for Gather-and-Reduce On Near-Memory Accelerators***
Aman Sinha, Pei-Yi Liu, Yuhao Fang and Jhih-Yong Mai, Bo-Cheng Lai (National Yang Ming Chiao Tung University, Taiwan)

15:25 ***MAO: Memory Architecture Obfuscation***
Sun Tanaka and Shinya Takamaeda-Yamazaki (The University of Tokyo, Japan)

Tuesday, December 19, 2023. Time: 14:40 – 15:40 (GMT+8)

B4: Emerging Machine Learning and Deep Learning Models: Theory & Applications – II.
Chair: Yoichi Tomioka (University of Aizu, Japan), Co-chair: Yue Zheng (The Chinese University of Hong Kong, Shenzhen, China)

Room: Room-B

14:40 ***Dynamic Hand Gesture Recognition Using Effective Feature Extraction and Attention-Based Deep Neural Network***
Abu Saleh Musa Miah (The University of Aizu, Japan); Jungpil Shin (University of AIZU, Japan); Md. Al Mehedi Hasan (Rajshahi University of Engineering and Technology, Bangladesh); Yuichi Okuyama (The University of Aizu, Japan); Nobuyoshi Asai (University of Aizu, Japan)

14:55 ***Decentralized Reinforcement Learning with FPGA Acceleration for Anomaly Detection in UAV Network***
Dylan R Tocci and Ruolin Zhou (University of Massachusetts Dartmouth, USA)

15:10 ***Generating Realistic Images with NeRF for Training of Autonomous Driving Network***
Shun Sugaya (University of Aizu, Japan); Yuichi Okuyama (The University of Aizu, Japan); Yuta Shintomi (Graduate School of University of Aizu, Japan); Ryota Kusano (University of Aizu Graduate School, Japan); Kohsuke Tanaka (The University of Aizu, Japan); Jungpil Shin (University of AIZU, Japan); Satoshi Nishimura (The University of Aizu, Japan)

15:25 ***A Lightweight Action Recognition Method for Deployable Embedded Devices for Human-Computer Interaction***
Nanjie Hu, Ningyu Wang, Jie Lin, Qinghao Fu and Benying Tan (Guilin University of Electronic Technology, China)

Tuesday, December 19, 2023. Time: 15:50 – 16:50 (GMT+8)

A5: Multicore/Manycore SoCs Programming & Architecture – II.
John Jose (Indian Institute of Technology Guwahati, India), Co-chair: Meisam Abdollahi (University of Victoria, Canada) TBC

Room: Room-A

15:50 ***A Near-Memory Dynamically Programmable Many-Core Overlay***
Mahmoud Ahmed Elshimy (German University in Cairo, Egypt); Veronia Iskandar and Diana Goehringer (Technische Universität Dresden, Germany); Mohamed Abd El Ghany (German University in Cairo & TU Darmstadt, Egypt)

16:05 ***A Low-Stall Methodology for an Interleaved Processor State Replication***
Fabian Kempf, Julian Hoefer, Tim Hotfilter and Juergen Becker (Karlsruhe Institute of Technology, Germany)

16:20 ***Accelerating Graph-Based SLAM through Data Parallelism and Mixed Precision on FPGAs***
Junfeng Wu (Shenyang University of Technology, China); Yuan He (Keio University, Japan & Shenyang University of Technology, China); Masaaki Kondo (Keio University, Japan)

16:35 ***Lifetime Estimation for Core-Failure Resilient Multi-Core Processors***
Sudam M Wasala, Sobhan Niknam, and Anuj Pathania (University of Amsterdam, The Netherlands); Clemens Grelck (Friedrich Schiller University Jena, Germany); Andy Pimentel (University of Amsterdam, The Netherlands)

Tuesday, December 19, 2023. Time: 15:50 – 16:50 (GMT+8)

B5: Parallel/Distributed, Grid, and Cloud Computing.
Chairs: Zhishang Wang (University of Aizu, Japan), Huakun Huang (Guangzhou University, China)

Room: Room-B

15:50 ***Privacy-stealing Approach in Distributed IoMT Systems***
Haoda Wang (University of Aizu, Japan); Lingjun Zhao (Guangdong Polytechnic Normal University, China); Chen Qiu, Zhuotao Lian and Chunhua Su (University of Aizu, Japan)

16:05 ***A Novel Supervised Distributed Dictionary Learning based on Learned K-SVD for Image Denoising***
Chaoran Zhang and Huakun Huang (Guangzhou University, China); Lingjun Zhao (Guangdong Polytechnic Normal University, China); Chenkai Xu and Rui Zhao (Guangzhou University, China)

16:20 ***Reentrancy Vulnerability Detection Based on Graph Convolutional Networks and Expert Patterns***
LongTao Guo and Huakun Huang (Guangzhou University, China); Lingjun Zhao (Guangdong Polytechnic Normal University, China); Peiliang Wang and Sihui Xue (Guangzhou University, China)

16:35 ***Understanding the Performance Impact of Queue-Based Resource Allocation in Scalable Isaggregated Memory Systems***
Amit Puri and Abir Banerjee (IIT Guwahati, India); John Jose and Venkatesh Tamarapalli (Indian Institute of Technology Guwahati, India)

Tuesday, December 19, 2023. Time: 17:00 – 18:00 (GMT+8)

A6: Multicore/Manycore SoCs Programming and Architecture – III.
Chair: Kun-Chih Chen (National Yang-Ming Chiao Tung University, Taiwan), Co-chair: John Jose (Indian Institute of Technology Guwahati, India)

Room: Room-A

17:00 ***PortBlocker: Detection and Mitigation of Hardware Trojan through Re-routing and Bypassing***
Sachin Bagga and Ruchika Gupta (Chandigarh University, India); John Jose (Indian Institute of Technology Guwahati, India)

17:15 ***Systematic Construction of Deadlock-Free Routing for NoC Using Integer Linear Programming***
Shuang Liu (University of Stuttgart, Germany); Martin Radetzki (Universitaet Stuttgart, Germany)

17:30 ***Low-latency inter-domain communication on the Xen hypervisor***
Fabian Lesniak, Tanja Harbaum and Juergen Becker (Karlsruhe Institute of Technology, Germany)

17:45 ***Memory-efficient Edge-based Non-Neural Face Recognition Algorithm on the Parallel Ultra-Low Power (PULP) Cluster***
Mitul Sudhirkumar Nagar, Sayantan Maiti and Rahul Kumar (Sardar Vallabhbhai National Institute of Technology, India); Hiren Mewada (Prince Mohammad Bin Fahd University, Serbia); Pinalkumar Engineer (Sardar Vallabhbhai National Institute of Technology, Surat, India)

Tuesday, December 19, 2023. Time:17:00 – 18:00 (GMT+8)

B6: Emerging Machine Learning and Deep Learning Models: Theory & Applications – III. Chair: Wonjik Kim (National Institute of Advanced Industrial Science and Technology, Japan), Co-chairs: Incheon Paik, (University of Aizu, Japan), Qinglin Yang (Sun Yat-Sen University, China)

Room: Room-B

17:00 ***Interlinked Chain Method for Blockchain-Based Collaborative Learning in Vehicular Networks***
Zhishang Wang, Khanh N. Dang and Abderazek Ben Abdallah (University of Aizu, Japan)

17:15 ***Deep Learning-Driven Video Summarization on the Cloud: A Pathway to Efficient Storage and Quick Access***
Mahmoud Darwich (University of Mount Union, USA); Kasem Khalil (University of Mississippi, USA); Yasser Ismail (Southern University, USA); Magdy Bayoumi (University of Louisiana, USA)

17:30 ***Automatic Text Classification as Relevance Measure for Russian School Physics Texts***
Elijah Tomin (Kazan Federal University & Text Analytics Laboratory, Russia); Marina Solnyshkina and Elzara Gafiyatova (Kazan Federal University, Russia); Albina Galiakhmetova (Kazan State Power Engineering University, Russia)

17:45 ***Enhancing Deep Reinforcement Learning with Compressed Sensing-based State Estimation***
Shaswot Shresthamali and Masaaki Kondo (Keio University, Japan)

****End of Day 2****

Wednesday, December 20, 2023

Wednesday, December 20, 2023. Time: 9:00 – 10:00 (GMT+8)

K3:Mahdi Nikdast, Associate Professor, Colorado State University, USA. Title: "The Silicon Photonics Marathon: From Optical Interconnect to Computing and Memory!"

Chair: Michael Meyer (Eastern Washington University, USA)
Room: Room-A

Wednesday, December 20, 2023. Time: 10:10 – 11:10 (GMT+8)

A7: Machine Learning and Neuromorphic Computing for Edge and IoT.
Chair: Michael Meyer (Eastern Washington University, USA), Co-chair: Yasser Ismail (Southern University and A&M College, USA)

Room: Room-A

10:10 ***Design of a Nonvolatile-Neural-Network-Accelerator-Embedded Edge-IoT Device and Its Hardware Emulation***
Ken Sato (University of Aizu, Japan); Daisuke Suzuki (The University of Aizu, Japan)

10:25 ***Delay-optimized Topology Management of a Wirelessly Networked Disaster Area***
Michael C Meyer (Eastern Washington University, USA); Yu Wang (TriOrb, Japan)

10:40 ***A Novel Yield Improvement Approach for 3D Stacking Neuromorphic Architecture***
Nguyen Ngo Doanh and Khanh N. Dang (University of Aizu, Japan)

10:55 ***Fault-Tolerant Ensemble CNNs Increasing Diversity Based on Knowledge Distillation***
Shunsuke Koeda (The University of Aizu, Japan); Yoichi Tomioka (University of Aizu, Japan); Hiroshi Saito (The University of Aizu, Japan)

Wednesday, December 20, 2023. Time:10:10 – 11:10 (GMT+8)

B7: Multicore/Manycore SoCs Programming & Architecture – IV.
Chair: Trong-Thuc Hoang (University of Electro-Communications (UEC), Tokyo, Japan)

Room: Room-B

10:10 ***Distributed Data Logger Based on Dual-Core MCU in Motor Drive***
Duc Minh Tran and Joon-Young Choi (Pusan National University, Korea (South))

10:25 ***A Scalable JPEG Encoder on a Many-Core Array***
Thomas W Abbott and Bevan Baas (University of California, Davis, USA)

10:40 ***Universal 32/64-bit CGRA for Lightweight Cryptography in Securing IoT Data Transmission***
Sang Duong Thi (Nara Institute of Science and Technology, Japan); Hoai Luan Pham (NARA Institute

of Science and Technology, Japan); Le Vu Trung Duong (Nara Institute of Science and Technology, Japan); Diem Thi Tran (University of Information Technology, VNU-HCM, Vietnam); Ren Imamura (Nara Institute of Science and Technology, Japan); Quoc Duy Nam Nguyen and Thi Hong Tran (Osaka Metropolitan University, Japan); Yasuhiko Nakashima (Nara Institute of Science and Technology, Japan)

10:55 ***Modelling and Impact Analysis of Push Back Attack in 3D Bufferless Network on Chip***
Josna V R (Cochin University of Science and Technology & GEC Bartonhill, Trivandrum, India); Rose George Kunthara (School of Engineering, Cusat, India); Rekha James (Cochin University of Science and Technology, India); John Jose (Indian Institute of Technology Guwahati, India)

Wednesday, December 20, 2023. Time:14:00 – 14:55 (GMT+8)

T1: Tutorial: "E-Textile Pressure Sensors and Their Applications".
Lei Jing, Professor, University of Aizu, Japan

Room: Room-A

Wednesday, December 20, 2023. Time:15:10 – 16:10 (GMT+8)

A8: Multicore/Manycore SoCs Applications & Designs – II.
Chair: Michael Meyer (Eastern Washington University, USA), Tanja Harbaum (Karlsruhe Institute of Technology (KIT), Germany)

Room: Room-A

15:10 ***Autonomous Driving Robot Using FPGA and BNN with Random Forest***
Yasuyuki Suzuki (University of Aizu, Japan); Shogo Semba (The University of Aizu, Japan); Yoichi Tomioka (University of Aizu, Japan); Hiroshi Saito (The University of Aizu, Japan)

15:25 ***Implementation of Physics Informed Neural Networks on Edge Device***
T. Hui Teo (Singapore University of Technology and Design, Singapore); I-Chyn Wey (Chang Gung University, Taiwan); Xuezhi Zhang and Maoyang Xiang (Singapore University of Technology and Design, Singapore)

15:40 ***A Many-core Architecture for an Ensemble Ternary Neural Network Toward High-Throughput Inference***
Ryota Kayanoma, Akira Jinguji and Hiroki Nakahara (Tokyo Institute of Technology, Japan)

15:55 ***Selective Pruning of Sparsity-Supported Energy-Efficient Accelerator for Convolutional Neural Networks***
T. Hui Teo, Chia-Chi Liu, and Xuezhi Zhang (Singapore University of Technology and Design, Singapore); I-Chyn Wey (Chang Gung University, Taiwan)

Wednesday, December 20, 2023. Time:15:10 – 16:10 (GMT+8)

B8: Neuromorphic Computing Systems & AI on Edge.
Chairs: Khanh N. Dang (University of Aizu, Japan), Daisuke Suzuki (The University of Aizu, Japan)

Room: Room-B

15:10 ***First steps towards micro-benchmarking the Lava-Loihi neuromorphic ecosystem***
Walter Gallego Gomez (Politecnico di Torino – DIST, Italy); Andrea Pignata, Riccardo Pignari, Vittorio Fra and Enrico Macii (Politecnico di Torino, Italy); Gianvito Urgese (Politecnico Di Torino, Italy)

15:25 ***Review of open neuromorphic architectures and a first integration in the RISC-V PULP platform***
Michelangelo Barocci (Politecnico di Torino – DIST, Italy); Vittorio Fra and Enrico Macii (Politecnico di Torino, Italy); Gianvito Urgese (Politecnico Di Torino, Italy)

15:40 ***A Highly Accurate and Parallel Vision MLP FPGA Accelerator based on FP7/8 SIMD Operations***
Mari Yasunaga, Junnosuke Suzuki, Masato Watanabe, Kazushi Kawamura, Thiem V. Chu, Jaehoon Yu, and Masato Motomura (Tokyo Institute of Technology, Japan)

15:55 ***TensorRT Implementations of Model Quantization on Edge SoC***
Yuxiao Zhou (Texas State University, USA); Zhishan Guo (North Carolina State University, USA); Zheng Dong (Wayne State University, USA); Kecheng Yang (Texas State University, USA)

Wednesday, December 20, 2023. Time:16:20 – 17:20 (GMT+8)

A9: Multicore/Manycore SoCs Programming & Architecture – V.
Chair: Hiroki Nakahara (Tohoku University, Japan), Co-chair: Razaidi Hussin (Universiti Malaysia Perlis, Malaysia)

Room: Room-A

16:20 ***Low-cost Low-Power Implementation of Binary Edwards Curve for Secure Passive RFID Tags***
Manh-Hiep Dao (VNU Information Technology Institute, Vietnam); Xuan-Tu Tran (Vietnam National University, Hanoi, Vietnam); Vincent Beroulle and Yann Kieffer (University of Grenoble Alpes, France); Duy-Hieu Bui (Vietnam National University, Hanoi, Vietnam)

16:35 ***Mitigating Test-Induced Yield-Loss by IR-Drop-Aware X-Filling***
Shiling Shi, Stefan Holst, and Xiaoqing Wen (Kyushu Institute of Technology, Japan)

16:50 ***Modelling Peripheral Designs using FSM-like Notation for Complete Property Set Generation***
Endri Kaja and Nicolas Gerlin (Infineon Technologies AG & Rheinland-Pfälzische Technische Universität Kaiserslautern-Landau, Germany); Keerthikumara Devarajegowda (Rheinland-Pfälzische Technische Universität Kaiserslautern-Landau, Germany); Wolfgang Ecker (Infineon Technologies AG, Germany)

17:05 ***Novel March WY Approach for Dynamic Fault Detection in Memory BIST***
Wan Ying Loh and Razaidi Hussin (Universiti Malaysia Perlis, Malaysia); Weng Fook Lee (Emerald Systems, Malaysia); Norhawati Ahmad (Universiti Malaysia Perlis, Malaysia); Aiman Zakwan Jidin (Universiti Malaysia Perlis & Universiti Teknikal Malaysia Melaka, Malaysia); Nor Azura Zakaria (UST Global Sdn Bhd, Malaysia)

Wednesday, December 20, 2023. Time: 16:20 – 17:20 (GMT+8)

B9: Emerging Machine Learning and Deep Learning Models: Theory & Applications – IV. Chair: Masato Motomura (Tokyo Institute of Technology, Japan), Co-Chair: Wonjik Kim (National Institute of Advanced Industrial Science and Technology, Japan)

Room: Room-B

16:20 ***GeMP-BNN: High-Performance Sampling-Free Bayesian Neural Network Accelerator with Gaussian Error Moment Propagation***
Yuki Hirayama, Kengo Suga and Shinya Takamaeda-Yamazaki (The University of Tokyo, Japan)

16:35 ***Recursive Algorithm FIR Filter Quantization and Low-Cost Structure Optimization Design Based on MATLAB and Simulink***
Zixia Shang (University of New South Wales (UNSW) & Siemens, China)

16:50 ***Exploring Discriminability of Categorical Anchors for Heterogeneous Domain Adaptation***
Yan Song and Junchu Huang (Research Institute of China Telecom Corporation Ltd, China)

17:05 ***Appropriate Graph-Algorithm Selection for Edge Devices Using Machine Learning***
Yusuke Fukasawa, Kazuhiko Komatsu, Masayuki Sato and Hiroaki Kobayashi (Tohoku University, Japan)

****End of Day 3****

Thursday, December 21, 2023

Thursday, December 21, 2023. Time: 9:00 – 10:00 (GMT+8)

Keynote 4: Steven Fong, Managing Director, AMD South Asia Pacific Sales, Singapore. Title: "Accelerating Silicon technology to deliver the exponential growth in Compute"

Room: Room-A
Chair: Tee Hui Teo (Singapore University of Technology and Design, Singapore)

Thursday, December 21, 2023. Time:10:10 – 11:10 (GMT+8)

A10: Embedded Multicore/Manycore SoC Architectures and Programming. Chair: Pham Hoai Luan (Nara Institute of Science and Technology, Japan), Co-chair: Kasem Khalil (University of Mississippi, USA)

Room: Room-A

10:10 ***Using Multiple Clocks in Highlevel Synthesis to Overcome Unbalanced Clock Cycles***
Yosi Ben-Asher and Ibrahim Qashqoush (University of Haifa, Israel)

10:25 ***Enhancing Anonymity in NoC Communication to Counter Traffic Profiling by Hardware Trojans***
Syam Sankar (Indian Institute of Technology Guwahati, India); Ruchika Gupta (Chandigarh University, India); John Jose and Sukumar Nandi (Indian Institute of Technology Guwahati, India)

10:40 ***Parallel Verification in RISC-V Secure Boot***
Akihiro Saiki and Yu Omori (Waseda University, Japan); Keiji Kimura (Waseda Univ, Japan)

10:55 ***High-efficiency Reconfigurable Crypto Accelerator Utilizing Innovative Resource Sharing and Parallel Processing***
Le Vu Trung Duong (Nara Institute of Science and Technology, Japan); Hoai Luan Pham (NARA Institute of Science and Technology, Japan); Thi Hong Tran (Osaka Metropolitan University, Japan); Sang Duong Thi, Ren Imamura, Akabe Tomoya and Yasuhiko Nakashima (Nara Institute of Science and Technology, Japan)

Thursday, December 21, 2023. Time:10:10 – 11:10 (GMT+8)

B10: Performance Optimization and Auto-Tuning of Software on Multicore/Manycore Systems (POAT2023). Chair: Kazuhiko Komatsu (Tohoku University, Japan)

Room: Room-B

10:10 ***Scale Up while Scaling Out Microservices in Video Analytics Pipelines***
Priscilla Benedetti (University of Perugia, Italy & Vrije Universiteit Brussels, Belgium); Giuseppe Coviello (NEC Laboratories America, USA); Kunal Rao (NEC Laboratories America Inc., USA); Srimat Chakradhar (NEC Research Labs, USA)

10:25 ***Performance of precision auto-tuned neural networks***
Quentin Ferro, Stef Graillat, Thibault Hilaire and Fabienne Jézéquel (Sorbonne Université, CNRS, LIP6, France)

10:40 ***A Constraint Partition Method for Combinatorial Optimization Problems***
Makoto Onoda, Kazuhiko Komatsu, Masahito Kumagai, Masayuki Sato and Hiroaki Kobayashi (Tohoku University, Japan)

10:55 ***Sparse Matrix-Vector Multiplication with Reduced-Precision Memory Accessor***
Daichi Mukunoki (RIKEN Center for Computational Science, Japan); Masatoshi Kawai (Nagoya University, Japan); Toshiyuki Imamura (RIKEN & Advanced Institute for Computational Science, Japan)

Thursday, December 21, 2023. Time:11:50 – 12:00 (GMT+8)

C: Closing session

Room: Room-A

****End of Day 4****