3-10-2 On-Board Data Processing Part Time-Comparison-Equipment Processing Unit (TCE-PRO)

KIUCHI Hitoshi, IMAE Michito, TAKAHASHI Yasuhiro, GOTOH Tadahiro, NAKAGAWA Fumimaru, FUJIEDA Miho, and HOSOKAWA Mizuhiko

In satellite positioning systems, such as the Global Positioning System (GPS), the receiver's position is calculated from the measured pseudo-range of the received radio signal. This signal is generated by the satellite based on its on-board atomic clock. Any error in the on-board clock directly affects the pseudo-range. Synchronization between the clocks on-board satellites and clocks on earth is thus indispensable for the development of next-generation systems. The goal of our research is to establish a precise method for comparing the time between earth and satellite clocks. The time-comparison-equipment processing unit (TCE-PRO) on-board Engineering Test Satellite VIII (ETS VIII) functions as the TCE-control unit; it controls data acquisition as well as digital data processing. It calculates the pseudo-ranges and instrumental delay from the code phases and carrier phases of a combined IF signal (the received signal, the transmitted signal, and the delay calibration signal), enabling the time to be synchronized between earth and satellite clocks.

Keywords
ETS-VIII, Satellite positioning, Time comparison/transfer, Digital signal processing, Delay lock loop (DLL), Costas loop

1 Introduction

A satellite positioning system determines a global location based on the difference between a time on the received signal generated by an onboard satellite clock and a ground reception time; it is thus essential to synchronize satellite and ground-based clocks. Time-control equipment (TCE) [1][2] is used to perform this synchronization. This paper describes the digital processing unit of a particular TCE device, referred to as the "TCE-PRO." The TCE-PRO measures the phase of various signals: the reference signal from a HAC (High Accuracy Clock), the signal transmitted from the satellite, a signal received from the ground, and the instrument delay calibration signal in the in-orbit satellite station that is sent from the TCE-RF unit via the HAC, permitting calculation of the amount of delay in each signal, which in turn enables synchronization of ground and satellite time. In order to compensate for instrument delay, the circuit is constructed to apply digital processing at all stages, and signals are digitized immediately following input. Frequency conversion and demodulation are also performed via digital processing.

2 Functions of TCE-PRO

We will first briefly discuss the various functions of the TCE-PRO. Fig.1 shows a block diagram of the device.

- Control of TCE unit (TCE control)

Transmission and reception of data to and from the data bus RIM of the main body of the satellite by RS422 serial transmission; control of the RF unit and determination of RF unit status

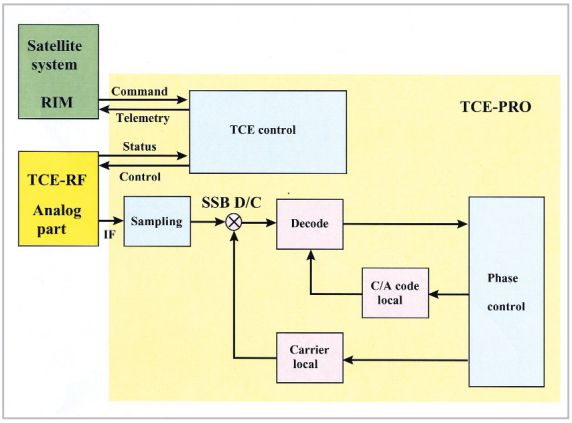


Fig.1 *Overall block diagram*

- Acquisition of observed signal (Sampling & SSB D/C)

The overall TCE-PRO system is based on digital signal processing in order to eliminate instrument delay. It is common in frequency conversion (e.g., DC down-conversion) to place a filter before a mixer for SSB (single sideband) conversion; however, circuit size is limited in the available satellite components, precluding the use of an FIR filter or similar component. Therefore, an IRM (Image Rejection Mixer) system was adopted. IRM digital frequency conversion is also useful in avoiding group-delay frequency errors attributable to the use of SSB filters. Frequency conversion was performed in two steps: initial coarse conversion, followed by fine conversion. An NCO (Numerically Controlled Oscillator), a digital version of a VCO (Voltage Controlled Oscillator), was adopted for the local oscillators.

- Digital signal processing

Generally, code phase detection entails (among others) delay detection, along with synchronous or asynchronous delay lock loops (DLL), while carrier phase detection involves elements such as second harmonic generation or the Costas loop. To detect code phase and carrier phase using the TCE, code tracking featuring synchronous DLL was adopted, with carrier tracking incorporating the Costas loop. Both loops are controlled by a CPU (phase control); an error signal is provided both to the code tracking (C/A code) NCO and to the local oscillator (carrier); this signal is then used to control the loops. Code phase and the carrier phase are acquired based on the NCO phase or the error signal phase.

2.1 Control of TCE unit

The basic functions of the control timing system are as follows.

- Command/telemetry management between control timing system and satellite system (RIM)
- Input/output of status (e.g., lock status) via parallel I/O; control of the RF unit (TCE-RF)
- C/A code generation based on software-specified SV# for internal satellite processing, independent of the digital signal processing unit
- Timing management

2.2 Acquisition of observed signal

The analog signal from the TCE-RF unit is sampled at 20.46 Msps. When acquiring the observed signal, two Doppler components are taken into consideration: the component resulting from precise Doppler tracking of the satellite, and the fixed large Doppler component acting as a basic component. Although it is possible to compensate for both components at once, it is an antithetical concept for NCO, between generating a high-frequency signal and a high-resolution signal at lower frequencies; therefore, we adopted a method of dual-stage frequency conversion. The NCO is used for the first and second local oscillators. The TCE-RF has the simultaneous generation of SIN and COS signals in order to compose an IRM, resulting in SSB conversion. Fig.2 illustrates the principle behind IRM frequency conversion with reference to an analog signal configuration. In the figure, the first NCO removes a basic component of the frequency, and the second NCO is used for precise tracking of the carrier. These local signals function as an element of the Costas loop described later.

2.3 Digital signal processing

The code phase and the carrier phase are measured using digital signal processing.

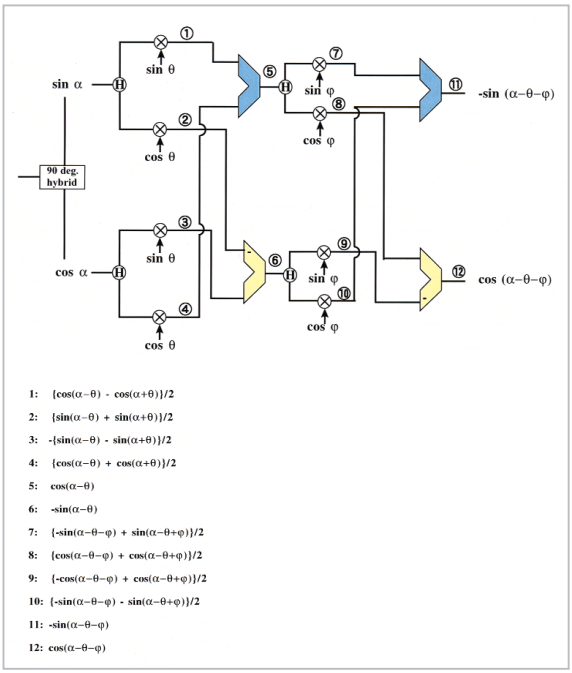


Fig.2 *Principle of IRM D/C*

2.3.1 Delay lock loop (DLL) for code phase synchronization

To obtain the phase of the code signal (using the code chip), delay detection method involves correlation integration of the input signal with a half-clock delayed input signal. This method does not require the use of a code. However, we adopted the DLL method, incorporating deciding using a code signal; this method is particularly advantageous in terms of SNR (Signal to Noise Ratio). Fig.3 shows a block diagram of the DLL. The DLL circuit performs correlation integration of the three kinds of C/A codes generated in the receiver (zero delay: "typical;" half-clock lag: "lag;" half-clock lead: "lead") and the input signal to measure the code delay. Several

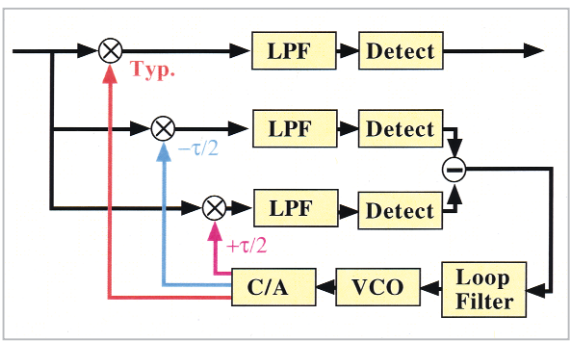


Fig.3 *DLL block*

kinds of DLLs are available, including asynchronous (non-coherent) DLL, t-dither type DLL, and synchronous (coherent) DLL. The various features of these DLLs are shown below.

(i) Asynchronous DLL

Asynchronous DLL employs a system in which an input signal is amplitude detected using code signals shifted from the input signal by a half-clock relative to the code. This type of DLL is referred to as "asynchronous" because processing is performed without compensation for the carrier component.

(ii) τ-dither type DLL

A τ-dither type DLL is a circuit integrating a mixer (EXOR) with one asynchronous DLL with a half-clock lag and another with a half-clock lead, a narrow-band bandpass filter, and an amplitude detector, all within a single device. This DLL toggles sequentially between the half-clock lag code and the half-clock lead code and adjusts the output of the amplitude detector accordingly. In this manner the electrical characteristics and the delay of the asynchronous DLL of the half-clock lag circuit is rendered identical to that of the half-clock lead circuit.

(iii) Synchronous (coherent) DLL

Synchronous (coherent) DLL is equipped with a carrier tracking processing system (involving phase-synchronization demodulation) in a stage preceding the DLL circuit; the DLL circuit itself performs processing within the baseband.

The TCE-PRO features synchronous (coherent) DLL, configured such that the DLL is integrated with the carrier synchronization system using the Costas Loop. Each DLL is comprised of a processing system involving three circuits, each incorporating three kinds of codes (zero delay, half-clock lag, half-clock lead: typical, lag, lead), a mixer (EXOR), a narrow-band bandpass filter, and an amplitude detector. The mixer outputs a signal at a frequency that is twice the code-chip frequency when the DLL code and the receiving signal code are synchronized. Accordingly, the center bandpass frequency of the narrow-band fil-

ter (or loop filter) is twice the code-chip frequency.

We will now discuss the procedure for pulling the DLL phase (see Fig.4).

- When the code phase is shifted from the signal code by more than one clock, the amplitude detectors of the three circuits all feature zero output.
- When the code phase is shifted from the signal code by exactly one clock, non-zero output is produced in the amplitude detector by either the half-clock lag circuit or the half-clock lead circuit.
- When the code phase deviates from the signal code by less than one clock, non-zero output is produced in all of the amplitude detectors; further, when the code phase and the signal phase coincide, the difference in output between the half-clock lag circuit and the half-clock lead circuit is zero.

A code phase synchronization system is constructed using the signal corresponding to the output difference between the half-clock lag circuit and the half-clock lead circuit as a VCO (NCO) to generate a code or an error signal in the code shift register (zero seeking: the error signal is controlled such that the signal coincides with a zero crossing point). At this time, if there is a difference between the noise (assumed as white-noise) in the lag component and that in the lead component, a measured distance error will result, as shown at the bottom of Fig.4.

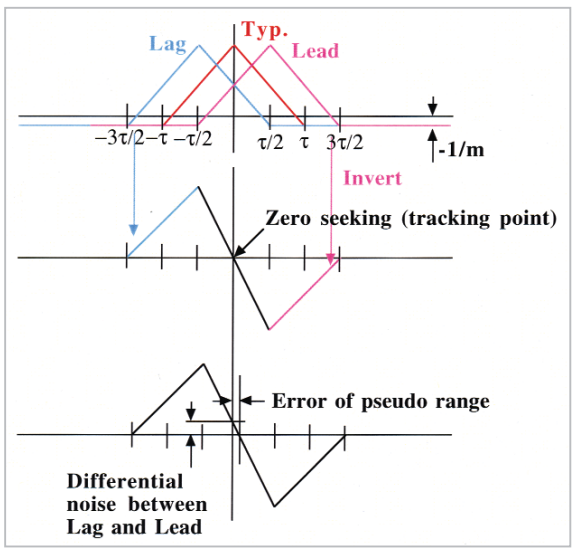


Fig.4 *Code correlation diagram*

Here, the input signal is assumed to correspond to the following expression.

$$S(t) = A \cdot C(t) \cdot D(t) \cdot \sin \omega t$$

where A: C/A code amplitude; $C(t)$: C/A code sequence; $D(t)$: navigation message code sequence; ω: carrier angular frequency. The received waveform at the TCE is expressed as follows, calculated using τ_d (propagation delay plus transmission-side time error).

$$S(t-\tau_d) = A \cdot C(t-\tau_d) \cdot D(t-\tau_d) \cdot \sin \omega (t-\tau_d)$$

The internally generated code pattern used to perform inverse spectrum spreading is expressed as follows, calculated using τ_0 (instrument delay including an internal time error etc.).

$$G(t-\tau_0) = C(t-\tau_0)$$

Through code demodulation, the combination of the received waveform and the internally generated code pattern is expressed as follows.

$$S(t-\tau_d) \cdot G(t-\tau_0) = A \cdot C(t-\tau_d) \cdot C(t-\tau_0) \cdot D(t-\tau_d) \cdot \sin \omega (t-\tau_d)$$

Here, when the phases of $C(t-\tau_d)$ and $C(t-\tau_0)$ coincide (i.e., when $\tau_d = \tau_0$), $C(t-\tau_d) \cdot C(t-\tau_0)$ becomes unity. At this point, within a variation time of $D(t-\tau_d)$, the right side of the expression is reduced to a sinusoidal wave ($\sin \omega(\tau_0 - \tau_d)$), indicating that power gathers in the carrier frequency from the spread spectrum band. On the other hand, when the phases are not in agreement, the expression alternates between +1 and -1, remaining in the spread spectrum state, with unresolved code spreading.

The correlation waveform of the DLL is detected as a set of several correlation waveforms subject to the multi-path effect; the resultant correlation waveform enables specific investigation of this effect. In this experiment, taking the features of a high-directivity ground-based antenna and those of the geostationary satellite into consideration, we concluded that the multi-path effect was in fact

negligible.

2.3.2 Costas loop for carrier phase synchronization

Carrier phase may be determined using a square-law detection method that does not require a code. In addition, the Costas loop makes use of a PLL (Phase Lock Loop) in a method of synchronous carrier regeneration that offers significant advantages in terms of SNR.

Fig.5 shows a block diagram of the Costas loop.

The input signal is multiplexed (by the first and second multipliers, found in the mixer) using VCO output signals featuring phases differing from that of the input signal by 90 degrees; the output signals are then passed through low pass filters (LPFs) to yield separate in-phase and quadrature components (normally referred to as the I and Q components). These signals are subject to multiplication by a third multiplier, and, after removal of the RF component, this output is used as the control signal of the VCO. With the third multiplexer, even when the signal is code division multiplexed, signals of the same code will be multiplied with the same timing, and thus only a carrier phase error will result.

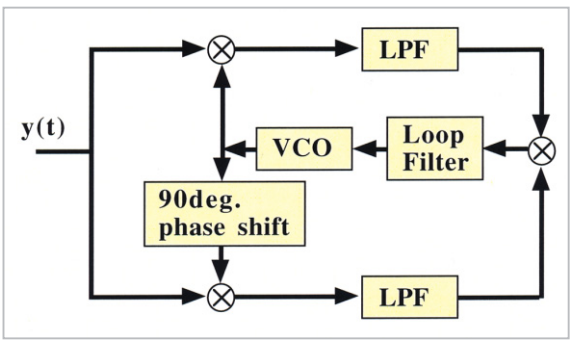


Fig.5 Costas Loop

A modulating signal y (t) input into the Costas loop can be expressed as follows.

$$y(t) = \sqrt{2}A \cdot D(t) \cdot cos(\omega_c t + \theta_i)$$

where A is the baseband signal amplitude, $D(t)$ is the baseband signal, ω_c is the carrier angular frequency, and θ_i is the carrier phase. The VCO outputs two signals whose phases differ from $y(t)$ by 90 degrees, $\sqrt{2}\,cos(\omega_c t + \theta_0)$ and $\sqrt{2}\,sin(\omega_c t + \theta_0)$; these signals are then mixed with $y(t)$. The RF components of the mixed signals are removed with filters to obtain $A \cdot D(t)cos(\theta_i - \theta_0)$ and $A(t)sin(\theta_i - \theta_0)$. The error signal of the Costas loop is obtained as a product of these components.

$$\frac{A^2 \cdot D^2(t)}{2} \sin 2(\theta_i - \theta_0)$$

In this multiplication operation, signals of the same codes are multiplied; thus phase error proportional to $2(\theta_i - \theta_0)$ can be obtained provided that $(\theta_i - \theta_0)$ is sufficiently small. In other words, phase ambiguity of 180 degrees is present in the reproduced carrier from the Costas Loop. This is due to the feature of the modulation method in which the PSK signal phase is changed by 180 degrees, in other words, due to the indeterminacy of the phase to which the carrier was phase synchronized.

Fig. 6 shows a block diagram which demonstrates the above principle.

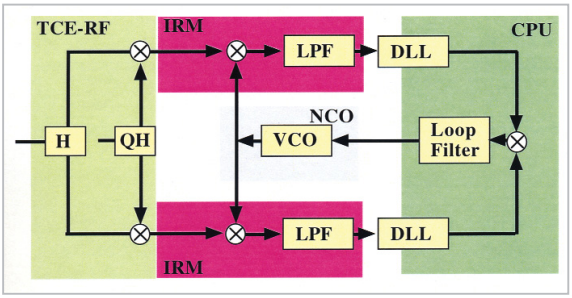


Fig.6 Signal processing system block diagram

3 Actual configuration of TCE-PRO

This chapter describes an actual circuit configuration. The TCE-PRO is composed of a CPU (which acquires the control signals and observed signals of the TCE) and digital signal processing units for transmitted, received, and delay-calibration signals; the equipment is constructed on a substrate of 240×250 mm. Fig.7 shows a schematic diagram of the overall configuration. Since the components of the CPU unit and the abovementioned digital signal processing units must all be constructed to

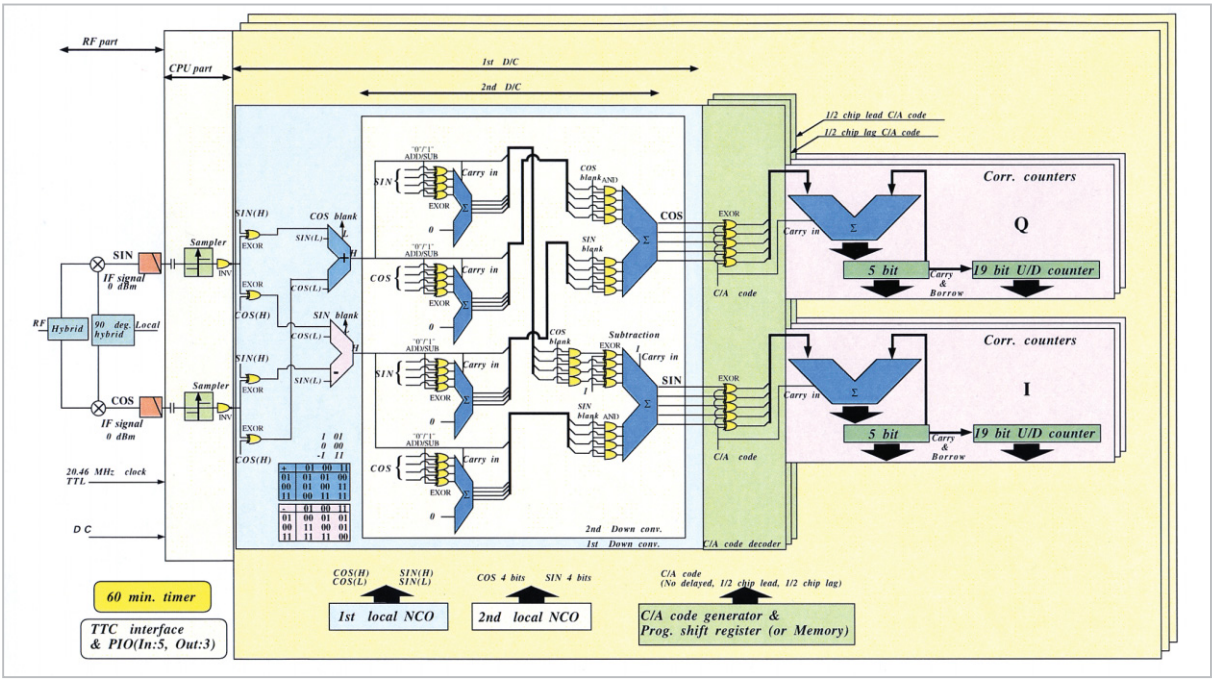


Fig.7 *Structure of TCE-PRO*

resist radiation, the high-performance, integrated parts suitable for use on the ground cannot be employed; lowering throughput and minimizing circuit size thus become prime concerns. The three digital signal processing units are compatible with one another, and each circuit adopts a whole-circuit FPGA (Field Programmable Gate Array) in its basic structure. Detection of the error phases of the DLL and the Costas loop and NCO control functions are performed by the CPU.

3.1 CPU unit

The CPU unit consists of a CPU motherboard, a telemetry system, a control timing system, a sampling system, and a C/A code generation system.

3.1.1 CPU motherboard

An 80 C286/12.5-MHz (clock reset control 82 C284) CPU is used that features proven radiation resistance. Memory space is formed with EPROM (16 bit × 32 kword), EEPROM (16 bit × 128 kword), and SRAM (16 bit × 128 kword). Taking damage due to vibration or the like at the time of satellite launch into consideration, alternate crystal reference clock systems are provided (system A and system B); one system can be replaced by the other automatically or by SM command. Further, in the event both systems fail, the 20.46-MHz RF unit signal is used as a clock reference. Changeover can be monitored via telemetry using an SD command. Moreover, the CPU motherboard is equipped with a watchdog timer to detect abnormal software states. The CPU is configured to select start-up software through the selection of EPROM or EEPROM.

3.1.2 Telemetry system

The telemetry system performs telemetry using the SM command (transmitted in units of 16 bits from the RIM) and the SD command (transmitting telemetry data to the RIM) by RS422 serial transmission to and from the RIM. Fig.8 shows a series of exchanges to and from the system.

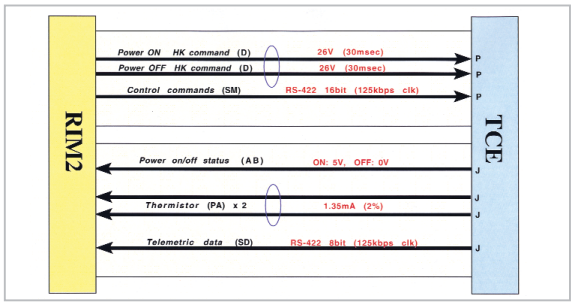


Fig.8 *TCE-RIM Command telemetry*

3.1.3 Control timing system

The control timing system is equipped with a time counter (00 min - 00 sec - 000 msec to 59 min - 59 sec - 999 msec), a PP (Parameter Period) cycle counter (0 sec - 000 msec to 9 sec - 999 msec), and a 24-bit interruption timer. When a given counter reaches its maximum value, it returns to zero and resumes counting. The PP cycle counter is programmed based on milliseconds, making periodic interruptions. All counters can be reset by external signals.

3.1.4 Sampling system

Analog signals (2.387 MHz ± 1.023 MHz, 0 dBm) differing from each other by 90 degrees and formed of a mix of transmitted, received, and delay-calibration signals supplied from the TCE RF unit, are fed to the sampling system, converted into a digital signal by sampling (1 bit, 20.46 Msps), and subsequently supplied to the different signal processing units. Although loss of coherence due to 1-bit quantization reaches 36% [3] even when the Nyquist rate is maintained, all of the loss is in amplitude information; there is no loss in phase information. The system is insensitive to amplitude variation, and is thus suitable for use as a system to acquire timing signals efficiently, as described in this paper. An anti-aliasing filter is installed in the output stage of the RF unit (TCE-RF). The digitized signal is passed along to the digital signal processing units (transmitted, received, and delay-calibration signal processing units) in the next stage.

3.1.5 C/A code generation system

The C/A code generation system generates a C/A code for demodulation based on the SV# specified by the software. The C/A code is output in synchronization with a 1.023-MHz timing signal from the CPU unit. This system shifts 1 bit of the code (and deletes/duplicates 1 bit). The system features a 20-bit variable shift register for fine-tuning phase when code searching, and is capable of adjusting phase at a resolution of 20.46 MHz. The system simultaneously generates three kinds of phase codes: “typical,” “1/2-bit lead,” and “1/2-bit lag” for the DLL circuit.

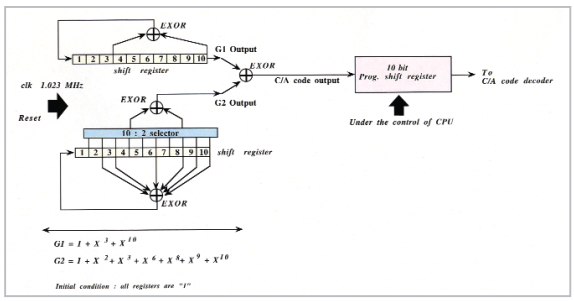


Fig.9 C/A Code generation

3.2 Digital signal processing unit (transmitted, received, and delay-calibration signal processing units)

The digital signal processing units (for transmitted, received, and delay-calibration signals) perform simultaneous measurement of the signal transmitted from the satellite, a signal received from the ground, the code of the satellite instrument delay calibration signal, and the carrier phase, based on a timing signal from the CPU unit. Measurement results are read by the CPU unit, processed, and output by telemetry.

3.2.1 Digital down converter

Since available CPUs and FPGAs featuring sufficient radiation resistance fall considerably short in terms of performance, we adopted the IRM method (rather than the initially envisioned SSB method, which entailed the use of FIR filters).

The NCO consists of a phase register (Φ), an additional phase register ($\Delta\Phi$), an adder, and a SIN/COS look-up table. Fig.10 shows the relevant block diagram. All bits of the phase resister are used to express phases of 0–360 degrees. $\Delta\Phi$ is controlled by the PP clock; a value of $\Delta\Phi$ (corresponding to the local frequency) is added to F every 1.023-MHz clock increment. An amplitude corresponding to this phase is read from the SIN/COS look-up table and is output. The value of the phase register is latched for each PP and rendered readable.

(i) First local signal

24-bit registers are used for the phase register and for the additional phase register of

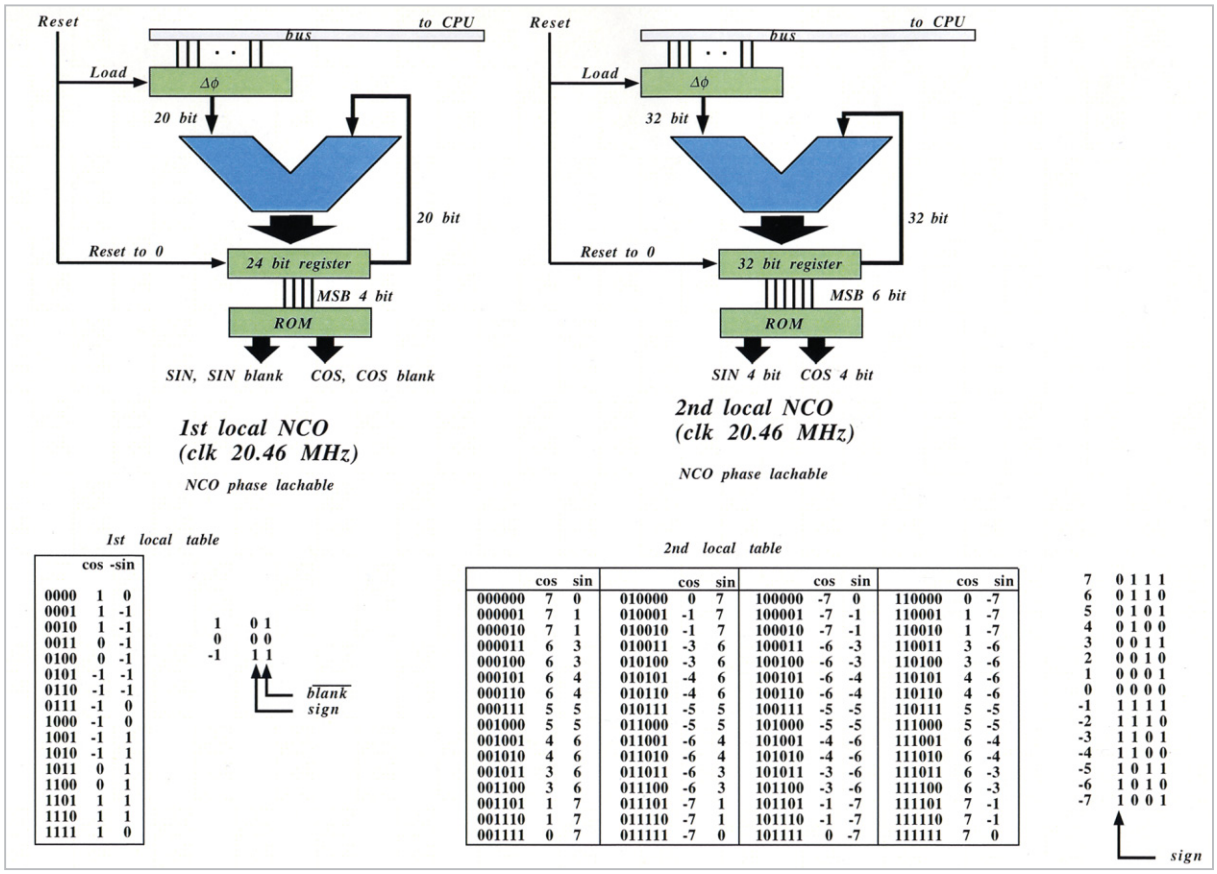


Fig.10 NCO Structure

the first local oscillator. The local (SIN/COS) signals are expressed with three-level approximation. The relationship between the three upper bits in the phase register and the SIN/COS lookup table is shown in the insert in Fig.10. The use of three-level approximation enables realization of a frequency conversion mixer with an EXOR logic circuit. Expression of a signal with three-level approximation (-1, 0, 1) requires two bits (Fig.11); output from the lookup table thus requires two bits: an MSB indicating sign and an LSB indicating amplitude. Here, output in which the LSB = 0 is defined as a blank signal that serves to halt operation of the final-stage integration circuit. Based on this principle, the register is required to send only one of the two bits of the initial down converter output to the second down converter, allowing for smaller circuit size.

(ii) Second local signal

A 32-bit register is used for the phase register and for the additional phase register of

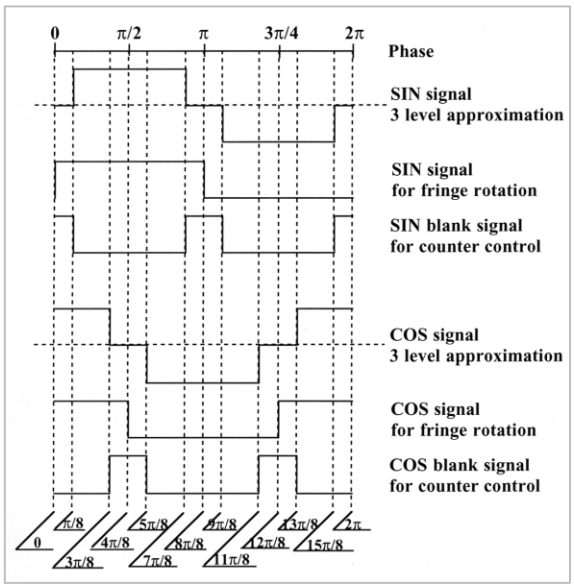


Fig.11 Three-level approximation

the second local oscillator. The local (SIN/COS) signals are expressed with 15-level approximation. The relationship between the upper 6 bits in the phase register and the SIN/COS lookup table is shown in the insert

in Fig.10.

In this system, the down converter can be changed to an up converter by changing the sign at one position, as is clear from the principle illustrated in Fig.2. Fig.12 shows the results of simulation for a case in which the frequency ratio (original signal to first local signal to second local signal) is set at 512:500:5 in the digital IRM. As indicated, the signals employed consist of the original signal (1 bit - 2 levels), the first local signal (2 bits - 3 levels), and the second local signal (4 bits - 15 levels). The upper two diagrams show the results of first-stage IRM frequency conversion (I: in-phase component, Q: quadrature component), with three-level output. The lower two diagrams show the results of second-stage IRM frequency conversion simulation at a frequency at which aliasing is likely to produce multiple images. In the figure, an image frequency component featuring a low level is anticipated at low frequencies. In principle it is best to pass the signal through a few taps of FIR filters downstream from the digital IRM.

3.2.2 Dual-correlation integration counter

The dual-correlation integration counter consists of a 24-bit up/down counter. Counters for the SIN component and for the COS component are prepared for each of three kinds of data: “typical,” “1/2-bit lead,” and “1/2-bit lag.” The up/down counter is controlled using 5-bit MSB code bits generated by demodulation (i.e., through correlation operation). This value is latched for each integration time and is read by the CPU. Once this value is fixed, the counter will be reset. Thus, phase difference can be arrived at by calculating the ATAN components using the SIN components and the COS components of the I and Q components of “typical.” This enables the same operations performed on the third multiplier of the Costa loop to be performed on the CPU.

Each of these circuits can support both synchronous and asynchronous operation; the specific method to be supported is determined through operational analysis. Moreover, the ability to rewrite the control software and FPGA software from the ground has also been considered.

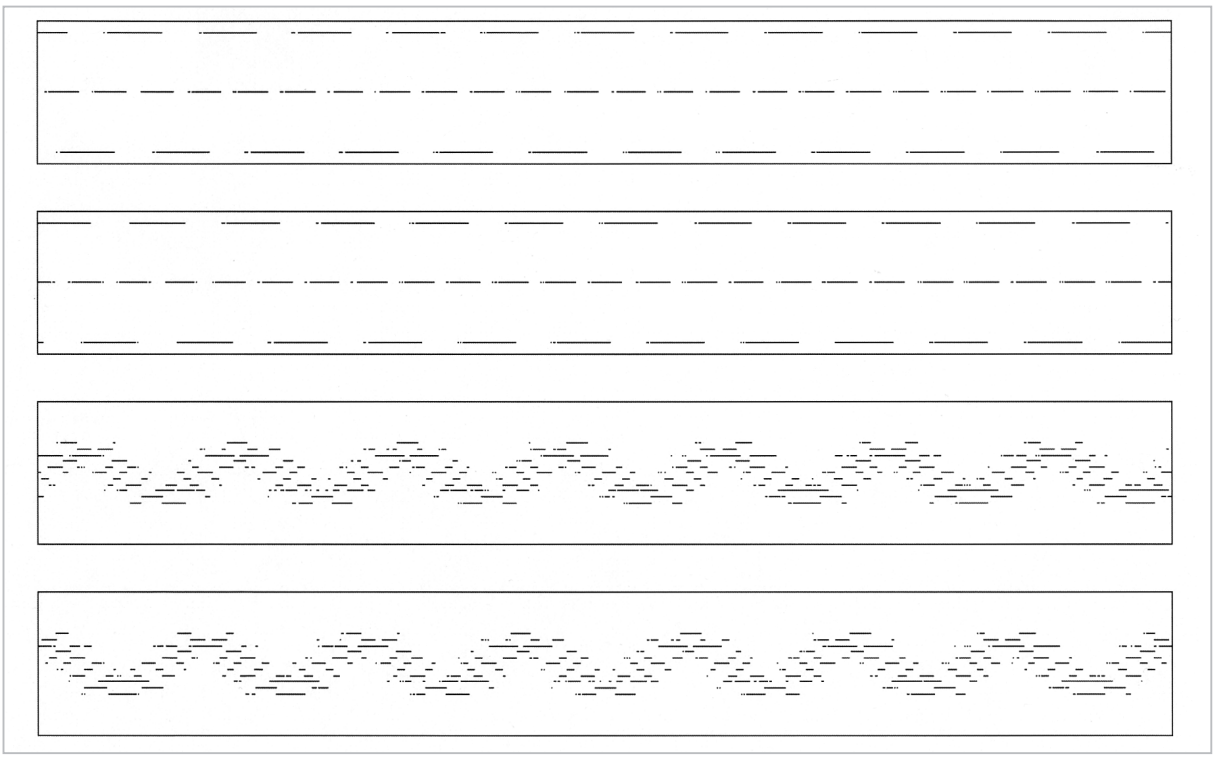


Fig.12 IRM simulation diagram

4 Acknowledgement

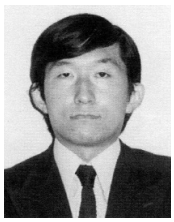
We are thankful to Mr. Hiroshima of the COSMO RESEARCH Corp., who manufactured the equipment used in the course of this research.

References

1 Y. Takahashi, "3-10-1 RF Part", This Special Issue of NICT Journal.

2 Y. Takahashi, M. Imae, H. Kiuchi, M. Hosokawa, M. Aida, T. Gotoh, H. Noda, S. Hama, and S. Kozono, "Experimental plan for time comparison equipment for ETS-VIII satellite," IEICE trans. B, Vol. J84-B, No.12, pp.2101-2107, 2001.12.

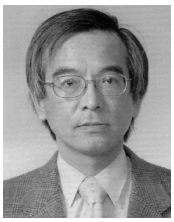
3 J.H.VanVleck and D.Middleton, "The spectrum of clipped noise", Proc. IEEE, Vol.54, No.1, pp.2-19, 1966.



***KIUCHI Hitoshi**, Dr. Eng.*

Senior Researcher, Optical Space Communications Group, Wireless Communications Division

Radio Interferometry, Optical Space Communication



IMAE Michito

Leader, Time and Frequency Measurements Group, Applied Research and Standards Division (present National Institute of Advanced Industrial Science and Technology)

Frequency Standard, especially on Precise Time Transfer

TAKAHASHI Yasuhiro

Senior Researcher, Time and Frequency Measurements Group, Applied Research and Standards Division

Satellite Communication, Satellite Positioning System

GOTOH Tadahiro

Researcher, Time and Frequency Measurements Group, Applied Research and Standards Division

GPS Time Transfer

***NAKAGAWA Fumimaru**, Ph. D.*

Research Fellow, Time and Frequency Measurements Group, Applied Research and Standards Division

Satellite Navigation, Satellite Time Transfer

***FUJIEDA Miho**, Ph. D.*

Research Fellow, Time and Frequency Measurements Group, Applied Research and Standards Division

Time Transfer, Satellite Navigation

***HOSOKAWA Mizuhiko**, Ph. D.*

Leader, Atomic Frequency Standards Group, Applied Research and Standards Division

Atomic Frequency Standards, Space Time Measurements