3-7 Nano-Gate Transistor — World's Fastest InP-HEMT —

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InP-based InGaAs/InAlAs high electron mobility transistors (HEMTs) which can operate in the sub-millimeter-wave frequency range (300 GHz – 3 THz) are key devices for future ultra-high-speed communications because of their high-frequency, low-noise performance. We succeeded in fabricating the world's shortest 25-nm-gate InP-HEMTs which exhibited a record current gain cutoff frequency (f_T) of 562 GHz. Moreover, we investigated the effect of device structures on their high frequency performance, and it was greatly improved by optimizing these structural parameters.

Keywords
Nano-Gate, Indium Phosphide (InP), High Electron Mobility Transistor (HEMT), Cutoff Frequency (f_T), Sub-millimeter-wave frequency range

1 Introduction

The frequency band from millimeter wave (30 to 300 GHz) to sub-millimeter wave (300 GHz to 3 THz) is presently underutilized, particularly in comparison with the commonly used optical waves and microwaves below and above this band. Nevertheless, this frequency region will prove critical in the future realization of ultra-high-speed wireless and optical communications networks. Effective utilization of this frequency range will require the development of ultra-high-speed transistors capable of taking full advantage of the excellent performance offered by the high-frequency sub-millimeter frequency range. We have recently developed a transistor with a record high cutoff frequency—in excess of 500 GHz—by optimizing the semiconductor crystal structure as well as the structure of the overall device.

This paper describes the process technology used for the fabrication of the world's fastest InP-based high electron mobility transistors (InP-HEMTs) and discusses the specific device structure required to ensure superb high-frequency performance.

2 Development of the world's fastest InP-HEMT

2.1 Fabrication of sub-50-nm gate InP-HEMT

When compared to conventional gallium-arsenide-based (GaAs) high electron mobility transistors (HEMTs), indium-phosphide-based (InP) HEMTs result in lower electron effective mass in the indium gallium arsenide (InGaAs) channel layer. InP-HEMTs also feature a relatively large conduction band offset (approximately 0.5 eV) between the channel layer and adjacent barrier layer (indium aluminum arsenide, InAlAs). Therefore, InP-HEMTs are characterized by high electron mobility, high electron saturation velocity, and high electron concentration. These characteristics are expected to lead to a marked increase in device speeds.

The schematic diagram in Fig. 1 shows the cross-sectional structure of an InP-HEMT.

The governing principles behind any improvement in the high-speed performance of an HEMT consist of reducing the traveling distance of electrons—the gate length—and increasing the traveling speed. We used electron beam (EB) lithography technology in an attempt to fabricate a T-shaped gate electrode with a gate length of less than 50 nm. Since the T-shaped gate enables the reduction of gate length while maintaining a large cross-sectional area, gate resistance can be minimized. For the electron beam (EB) lithography process, we used a tri-layer resist (ZEP/PMGI/ZEP) consisting of two types of electron beam (EB) resists. The top and middle layers were exposed simultaneously at a relatively low dose and then developed with a high-sensitivity developer. The bottom layer was then exposed at a relatively high dose and developed with a low-sensitivity developer. The resultant overhang structure is shown in Fig. 2a. Since the dimensions of the ultra-fine pattern on the bottom layer determine the gate length of the T-shaped gate, it is essential to fabricate, with high precision, an ultra-fine pattern of less than 50 nm. By optimizing the exposure and development conditions for the bottom-layer resist, we were able to achieve an ultra-fine pattern as narrow as 15 nm, and succeeded in accurate control of dimensions by simply adjusting the dose (Fig. 3).

Subsequently, we used a citric-acid-based aqueous solution for etching the cap layer (InGaAs) to create a gate-recess structure. In the final stage, we evaporated the gate-metal (Ti/Pt/Au) and lifted-off. Figure 2b shows a transmission electron microscope (TEM) image of the cross-section of the fabricated T-shaped gate with a gate length of 30 nm and a side-recess length of 50 nm.

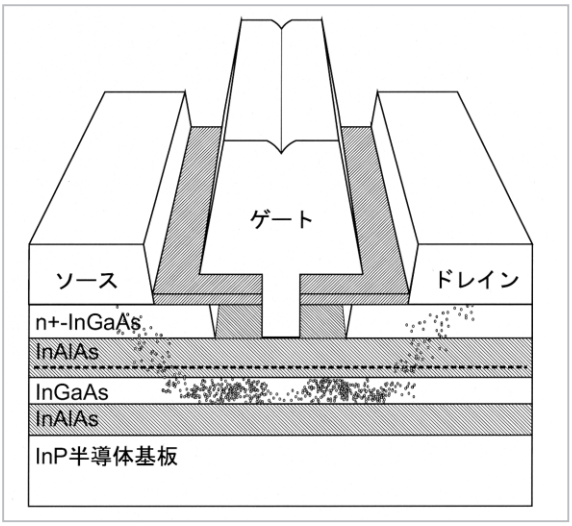

Fig.1 *Structure of InP-HEMT*

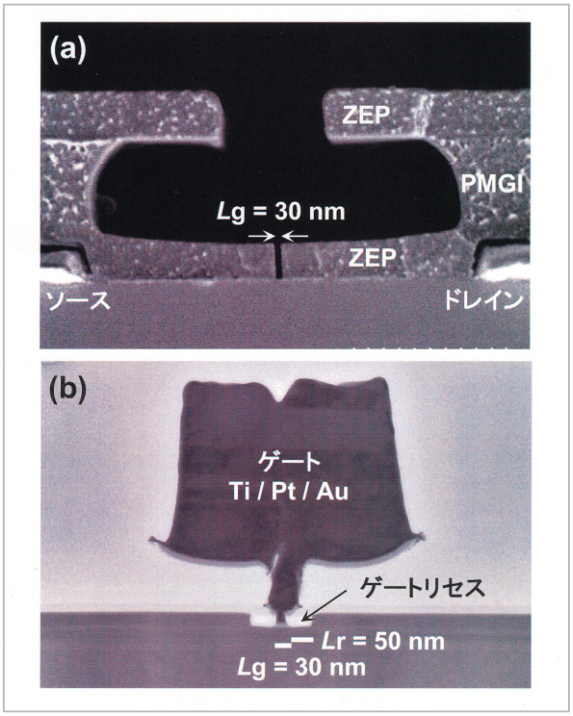

Fig.2 *(a) SEM cross-sectional image of tri-layer resist immediately after development; (b) TEM cross-sectional image of T-shaped gate*

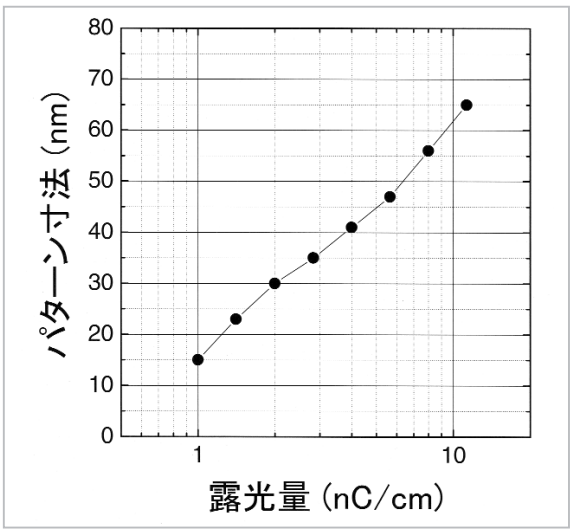

Fig.3 *Dose dependency of pattern dimension*

2.2 High-frequency performance of InP-HEMTs

Current gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) are often used as indicators of the high-speed characteristics of transistors. Specifically, f_T, which is expressed by $v/(2\pi L_g)$ (v: electron velocity, L_g: gate length), reflects the velocity and traveling distance of electrons within the transistor. Figure 4 shows the frequency dependency of the current gain ($|h_{21}|^2$) of an InP-HEMT with a gate length of 25 nm. The current gain at each frequency can be obtained by converting the S-parameter measured with a vector network analyzer (HP8510C). The cutoff frequency—the point at which the gain becomes zero—is determined by extrapolation based on a slope of -20 dB/decade using the measured data for frequencies of up to 50 GHz. The obtained f_T value of 562 GHz is the largest value ever reported for any transistor[1].

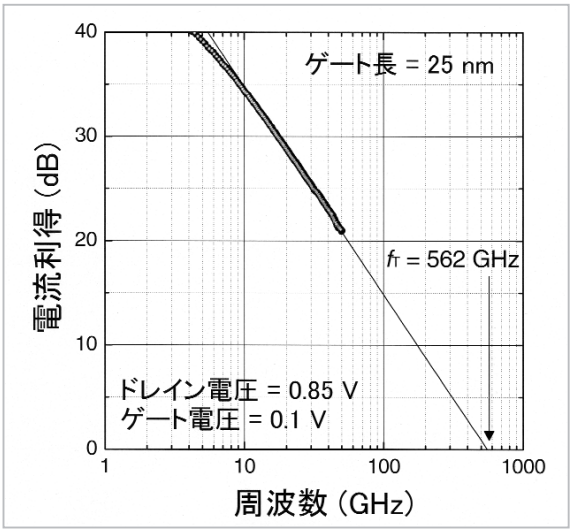

Fig.4 *Frequency dependency of current gain of pseudomorphic-channel InP-HEMT with gate length of 25 nm*

3 Effects of device structure on high-frequency performance

3.1 Gate-length dependence

Figure 5 shows the gate-length dependence of the f_T and transconductance (g_m) of an InP-HEMT (●)with lattice-matched $In_{0.53}Ga_{0.47}$ As channel layer[2]. The fabricated InP-HEMT featured a gate-channel distance of 13 nm, and the side recess length of the gate was 50 nm. This reduced gate length led to an observed increase in f_T. The value of f_T was 472 GHz when the gate length was 30 nm, and 400 GH when the gate length was 70 nm. The value of g_m was 1.25 S/mm when the gate length was 30 nm, and reached a maximum of 1.5 S/mm when the gate length was 100 nm. Compared to lattice-matched InP-HEMTs (□)[3] reported by other research groups, our HEMT's f_T and g_m values reflected 30% to 40% better performance. Comparison with a sample (■) featuring the same gate-channel distance but with a longer side recess length of 190 nm (equivalent to conventional HEMTs) indicates that the improvement in f_T and g_m is attributable to reduced side recess length.

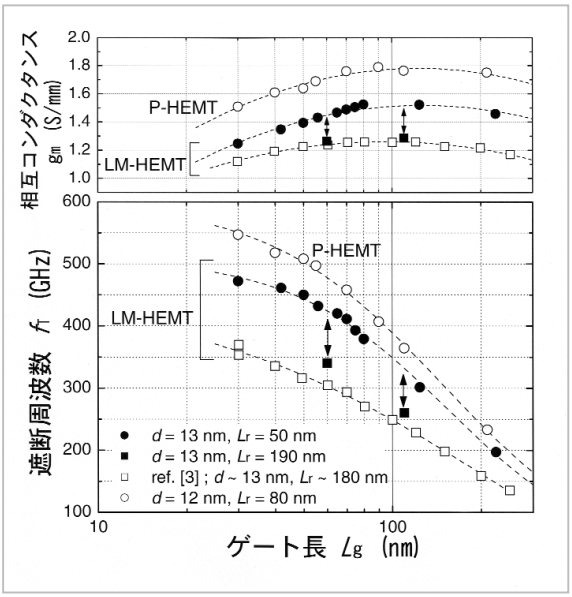

Fig.5 *Gate-length dependence of cutoff frequency and transconductance of InP-HEMT*

3.2 Asymmetric recess technology

As described above, the side recess length of the gate recess is believed to have a significant effect on the speed characteristics of the device. We therefore developed a process technology that enabled independent control of the side recesses length on the right and left sides of the gate electrode[4]. This simple, high-precision self-aligning process, outlined in Fig. 6, uses a conventional tri-layer resist.

The top and middle layers of this tri-layer resist are exposed and developed using conventional methods (a). A gate pattern and an ultra-fine slit pattern next to the gate pattern are then exposed and developed (b). The distance between the gate pattern and the slit is expressed by l, the slit size by $a \times b$, and the slit pitch by c. When the InGaAs layer is etched by a citric-acid-based etchant, a gate recess structure is formed. Since the etching action progresses not only through the gate pattern but also through the slit pattern, the recess shape becomes asymmetrical relative to the gate pattern (c). By providing an InP etch-stopper layer under the InGaAs layer, the etching can be stopped in the direction of depth. When the side etching length is r, the side recess lengths on the source and drain sides can be expressed by r, and $l + a + r$, respectively. Thus an asymmetric recess structure of a desired shape can be realized through appropriate setting of these parameters.

Furthermore, by reducing the slit pitch, c, to the level of r, the linearity of the etching edge on the drain side can be improved. In the final process, the gate metal is evaporated and deposited from the front side toward the back, at a tilted angle. This prevents the gate metal from depositing on the semiconductor surface below the slit, and allows for deposition only on the area below the gate pattern (d). Figure 7 shows a photo of a tri-layer resist immediately after recess etching and the cross-sectional image of an asymmetric recess T-shaped gate.

3.3 Recess-length dependency of f_T

To investigate the dependence of the high-speed characteristics of InP-HEMTs on side recess length, we evaluated the high-frequency performance of three types of asymmetric recess HEMTs with gate lengths of 60 nm fabricated using the method described above[5]. In the Type I sample, the recess length on the drain side was fixed at 50 nm, and the recess length on the source side was varied between 50 and 260 nm. In the Type II sample, on the other hand, the recess length on the source

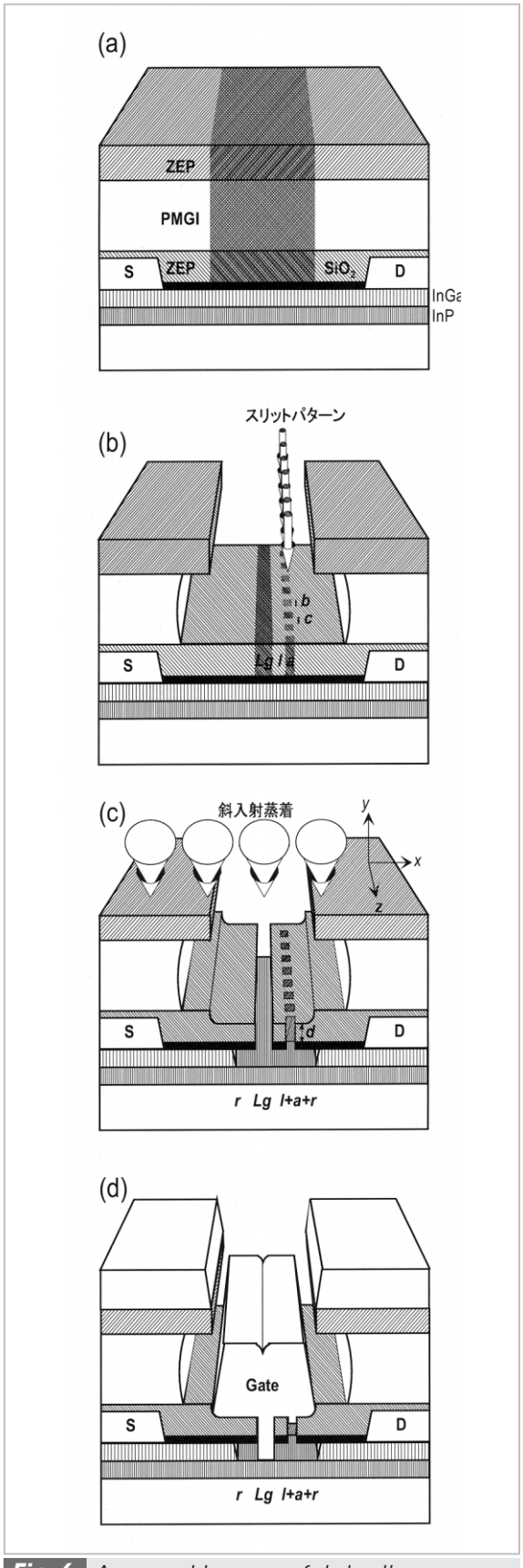

Fig.6 *Asymmetric recess fabrication process*

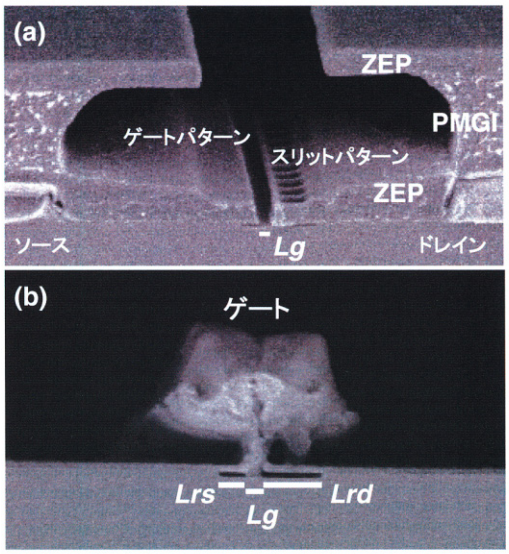

Fig.7 *(a) SEM cross-sectional image of tri-layer resist immediately after recess etching, (b) SEM cross-sectional image of asymmetric recess T-shaped gate*

side was fixed at 50 nm, and the drain-side recess length was varied between 50 and 260 nm. In the Type III sample, the recess lengths on both source and drain sides were varied simultaneously, from 50 to 260 nm. Figure 8 shows the recess-length dependence of f_T in each sample. In the Type I sample, f_T decreased gradually as the recess length on the source side became longer. By contrast, in the Type II sample, f_T decreased sharply as the recess length on the drain side became longer. The results for the Type III sample were similar to those seen in the Type II sample, but f_T values were slightly lower, given the longer recess length on the source side. These results indicate that the excellent high-speed characteristics of our InP-HEMTs are attributable largely to reduced recess length on the drain side.

Figure 9 shows the calculation results based on Monte Carlo simulations for two InP-HEMT structures. Both InP-HEMTs featured gate lengths of 60 nm and a fixed gate-source distance of 50 nm; however, the gate-drain distance was 50 nm in one sample and 260 nm in the other. The graph shows the distribution of electron velocity in the channel with the application of a drain voltage of 0.8 V and a gate voltage of -0.4 V. A clear velocity overshoot effect was observed below the gate, and peak velocity increased when the gate-drain distance was shortened. We believe that the shorter gate-drain distance increased the lateral electric field immediately under the gate, resulting in rapid acceleration of the electrons.

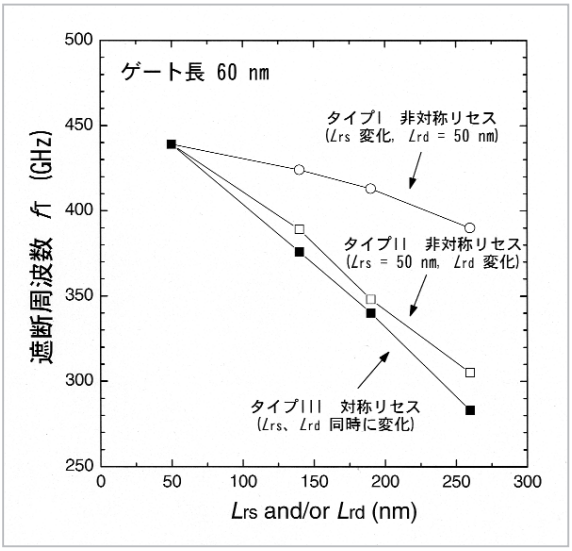

Fig.8 *Dependence of cutoff frequency on side recess length*

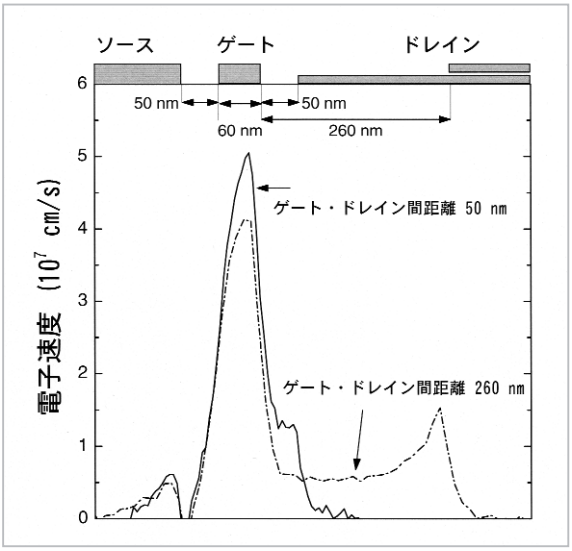

Fig.9 *Electron velocity distribution in InP-HEMT with gate length of 60 nm (calculation results based on Monte Carlo simulations)*

3.4 Increasing f_{max} with an asymmetric recess

Improvement of f_{max}, on the other hand, can be effectively achieved through an asymmetric

recess structure featuring a shorter recess length on the source side and a longer recess length on the drain side[4]. f_{max} can be expressed using equivalent circuit parameters in the following equation.

$$f_{max} = f_T / [4 g_d (R_s + R_i + R_g) + 2 (C_{gd}/C_{gs}) ((C_{gd}/C_{gs}) + g_m (R_s + R_i))]^{1/2} \quad (1)$$

As indicated by the equation, to increase f_{max}, it is necessary to increase f_T and g_m while at the same time reducing source resistance R_s, drain conductance g_d, and gate-to-drain capacitance C_{gd}. Figure 10 indicates the frequency dependence of the current gain ($|h_{21}|^2$) and Mason's unilateral gain (U_g) of two samples. Sample (a) featured a gate length of 60 nm, with recess lengths of 50 nm on the source and drain sides, while sample (b) had a gate length of 60 nm with recess lengths of 50 nm on the source side and 140 nm on the drain side. The f_T values were 439 GHz and 395 GHz, respectively. The long recess length on the drain side resulted in a reduced f_T value. On the other hand, the f_{max} values were 382 GHz and 500 GHz, respectively. Unlike the f_T values, f_{max} values showed significant improvement in the asymmetric recess sample. This improvement was due to the reduction of g_d and C_{gd} (i.e., below the values seen in the symmetric recess sample) while R_s was maintained at a low level.

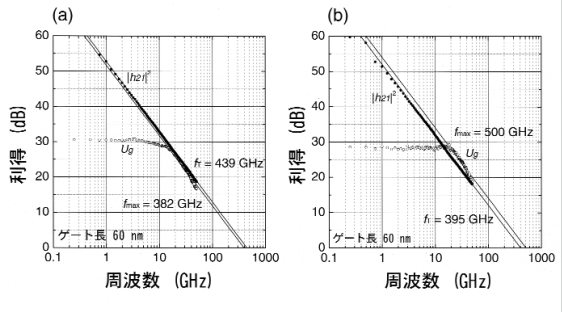

Fig.10 *(a) High-frequency performance of symmetric recess HEMT (L_{rs} = L_{rd} = 50 nm), (b) high-frequency performance of asymmetric recess HEMT (L_{rs} = 50 nm, L_{rd} = 140 nm)*

3.5 Effects of reduction of parasitic resistance

In an ultra-high-speed HEMT with f_T in excess of 500 GHz, parasitic resistance caused by the contact resistance (R_c) of the source and drain electrodes and by sheet resistance (R_{sh}) in regions on the source and drain sides of the gate cannot be neglected. Although R_s is 0.21 Ω mm in conventional structures, when the intrinsic g_m (g_{mi}) is assumed to be 2 S/mm, this value becomes 40% of 1/ g_{mi} (= 0.5 Ω mm).

We introduced a cap layer featuring a multi-layer structure with the aim of reducing R_s and R_d[6]. Figure 11 shows the structure of the HEMT thus fabricated. Using a 72-nm-thick InGaAs/InP/$In_{0.7}Ga_{0.3}As$ multi-layer structure with high Si doping level of 2×10^{19} cm^{-3} reduced R_{sh} to 22.8 Ω/sq. (compared to approx. 80 Ω/sq. seen in conventional structures). The use of a pseudomorphic $In_{0.7}Ga_{0.3}As$ layer as the top layer reduced R_c to 0.007 Ω mm (compared to 0.05 Ω mm in conventional structures). As a result, R_s was reduced to 0.15 Ω mm, representing a decrease of approximately 30%. Figure 12 shows the high-frequency performance of the fabricated pseudomorphic-channel $In_{0.7}Ga_{0.3}As$ HEMT with a gate length of 30 nm. The f_T was 547 GHz, and the f_{max} was 400 GHz. This qualified the component as the world's fastest HEMT, with both f_T and f_{max} exceeding 400 GHz. The circle in Fig. 5 indicates the gate-

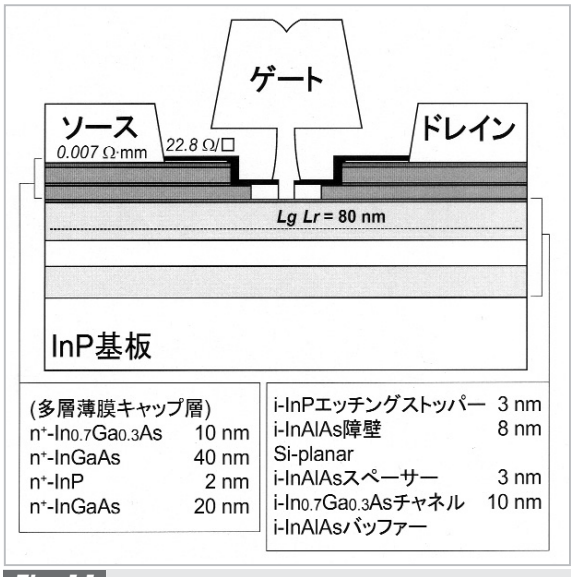

Fig.11 *Structure of pseudomorphic-channel InP-HEMT featuring multi-layer cap structure*

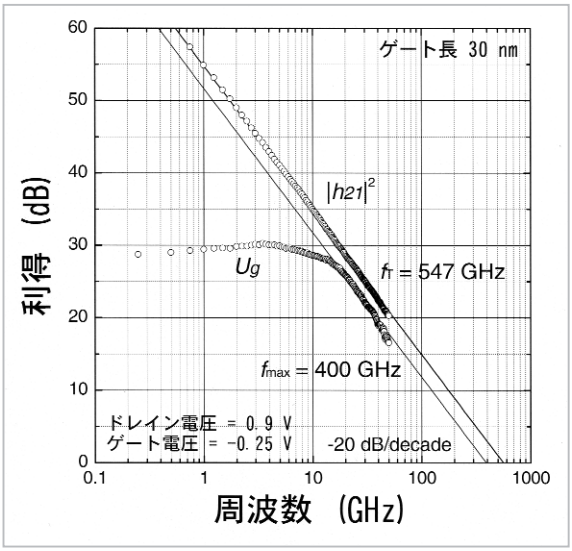

Fig.12 *High-frequency performance of pseudomorphic-channel InP-HEMT with gate length of 30 nm and multi-layer cap structure*

length dependence of f_T and g_m in this sample.

3.6 Reduction of channel width (one-dimensional channel InP-HEMT)

When the gate length becomes less than 100 nm, a phenomenon known as the "short-channel effect" becomes prominent, and the gate voltage can no longer effectively control the carrier. Figure 5 indicates that g_m is lower when the gate length is less than 100 nm. To mitigate this effect, we proposed using a narrower channel and providing bi-directional gate-voltage control of the carrier in the channel[7]. Figure 13 shows a schematic diagram of the narrow-channel InP-HEMT we fabricated and a TEM image of the narrow channel section of the actual device. Due to the waviness of the barrier layer thickness in the depthwise direction of the gate, electrons remain only in the channel layer below the thick barrier-layer section. This wavy structure was created using electron beam (EB) lithography technology and wet-etching technology. Electrons in the narrow channel are controlled by gate voltage not only in the vertical direction but also in the lateral direction; therefore, suppression of the degradation of g_m in a short gate becomes possible.

The graph in Fig. 14 was produced by plotting the values of drain current per narrow channel of an InP-HEMT fabricated with a gate length of 100 nm against the width of the narrow channel. The graph shows that the effective channel width varied according to gate voltage, indicating that carrier control in the lateral direction was functioning effectively. We expect that this structure will lead to improved electron transport property, based on the one-dimensional quantization of the channel, while also resulting in significant reduction in noise.

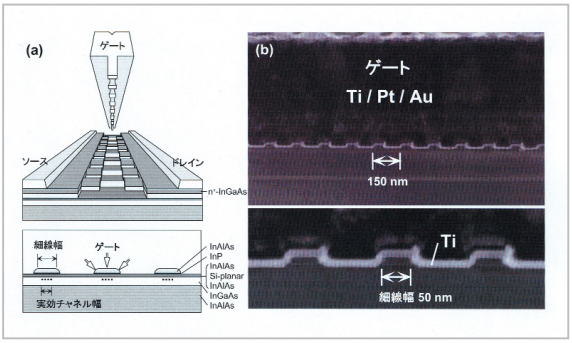

Fig.13 *(a) Structure of narrow-channel InP-HEMT; (b) TEM cross-sectional image of narrow channel*

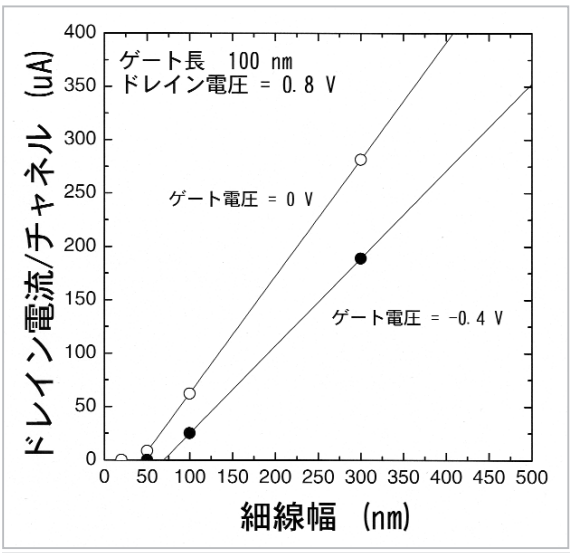

Fig.14 *Dependence of drain current on channel width for each narrow-channel-HEMT*

4 Summary

In the future, we plan to use the high-performance InP-HEMTs introduced in this paper to develop new millimeter-wave communica-

tions equipment technology for the 100-to-150 GHz frequency range, and to promote research and development of various practical millimeter-wave equipment such as ultra-broadband/ultra-low-noise amplifiers.

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