5-4 Ultra-fast Optical Processing Technology and its Application to Photonic Network

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Ultra-high speed all-optical label processing methods are proposed and experimentally demonstrated.These methods dramatically increase the label processing capability. Optical packet switch (OPS) systems and networks based on OPS nodes are expressed as an application of optical processing technologies. First 40 Gbit/s/port OPS prototype with all-optical label processor, optical switch, optical buffer, and electronic scheduler is expressed. The feasibility of OPS networks is verified by experimental demonstrations.

Keywords
Networks, Optical communications, Optical label processing, Optical packet switching, Prototype

1 Introduction

In the next generation optical network, high scalability and fine granularity will be strongly required in addition to broadband. Wavelength division multiplexing (WDM) technology has enabled broadband data transmission [1]. However, the granularity of a WDM light-path network is coarse. Although Internet protocol (IP) over generalized multi-protocol label switching (GMPLS) over WDM approach provides a fine granularity [2], its slower electronic processing, such as memory access for header analysis at IP routers, will be a bottleneck of a network. Optical processing technologies are needed for high-speed processing for broadband photonic network. We have proposed and experimentally demonstrated optical packet switching (OPS) networks based on optical label (i.e. code) processing, such as header analysis and label swapping [3][4]. Optical processing based OPS networks can provide high scalability, fine granularity and ultra high-speed hopping. Recently, in spite of immatureness of optical technology, many OPS systems have been developed because of its big merit [5]-[8]. Recently, we have developed 40 Gbit/s interface, all-optical label processing based OPS prototype with optical switch, optical buffer, and electronic scheduler [8]. This is the first OPS prototype with ultra-fast functions such as optical address-table lookup and transparent optical buffering.

An optical packet consists of a header and a payload data. The header has an *optical code-based label* [3][4][8][9][10][12] representing a destination node. In the label processor, a packet header label is analyzed all optically. All-optical label processing methods are represented in Fig. 1. We have investigated three different label-processing methods: (a) planner lightwave circuits (PLC) based correlators with binary phase shift keying (BPSK) code label [3][8], (b) multi-section fiber Bragg grating (FBG) based correlators with multi-wavelength label [4], and (c) a holographic multiple correlator with on-off keying (OOK) or BPSK label [9][10][12].In methods (a) and (b), a set of optical correlators works as a label bank, which holds optical labels correspond to the destination addresses in the routing table.

Label recognition is based on parallel optical correlation in the time and/or frequency domain between an input optical label and labels in the label bank. In the method (c), an angular multiplexed spectral hologram (AMSH) is used as a multiple correlator for input labels. An AMSH holds many optical labels correspond to the destination addresses and outputs correlation signals toward different angles due to input labels.

2 Optical code based label processing and switching

2.1 Network architecture and packet format

Figure 2 (a) represents proposed photonic network architecture. The network consists of edge nodes, optical cross connects (OXC), and OPS nodes. Edge nodes are connected with the local routers either in access networks or users' premises. OPS nodes are located in the photonic network as backbone routers. These packet switches can communicate with each other through OXC in core network. Packet-by-packet electrical processing is not performed. It will minimize transfer delay and support the high throughput of the nodes. Figure 2 (b) represents proposed optical packet format. A packet consists of header and payload data. We are using 200 Gchip/s, 8-chip, optical BPSK code label as a packet header involving a destination node address information. In the system, variable rate burst data is acceptable because of no O/E and E/O conversion to the data. To generate high-speed data, electric time domain multiplexing (ETDM) or optical time domain multiplexing (OTDM) technology is introduced. In any data rate cases, chip rate of the label is not changed. These time domain multiplexing technologies in OPS network is useful for making a shorter length packet and enhancement of a network scalability.

2.2 Label recognition and packet switching

As described in previous sub-section, an optical packet consists of a header and a data (see in Fig. 2(b)). The header has an optical code-based label of a destination node. In the OPS node, an optical packet is simply divided into two arms. In the label processing part, an optical label processor analyzes a packet header optically. All-optical label recognition method is represented in Fig. 3. In an optical

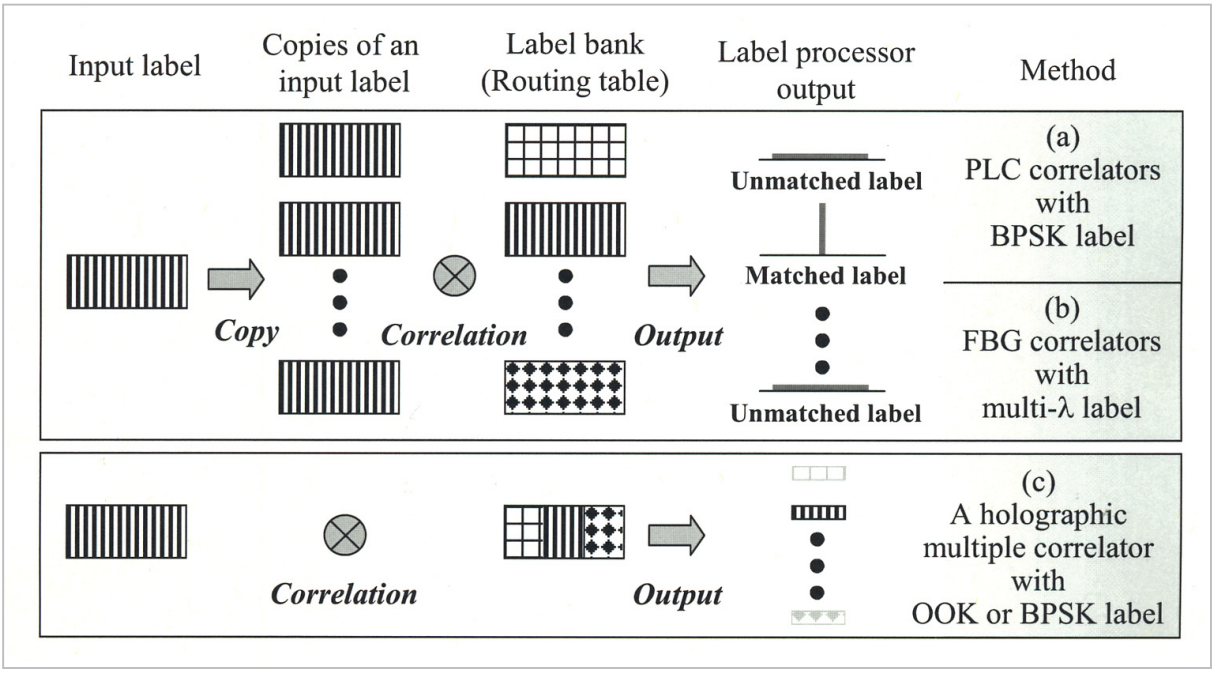

Fig.1 *All-optical label processing methods*

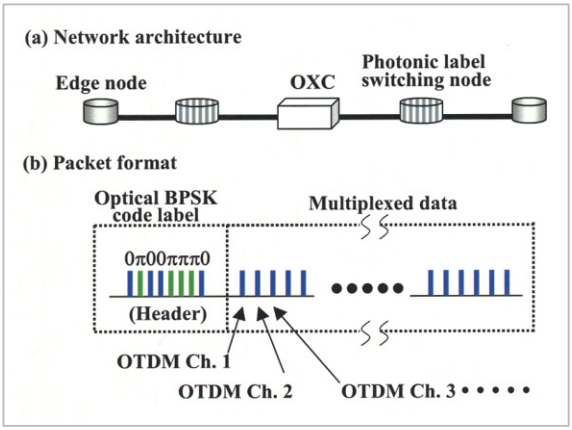

Fig.2 *(a) Network architecture and (b) packet format*

label processor, a set of optical correlators works as a label bank, which stores optical codes correspond to the destination addresses in the routing table. Label recognition is based on parallel optical correlation in the time domain between an input optical code and the codes in the label bank. Each correlator decodes the input label of each packet header and outputs the signal, which has high or low value at matched and unmatched cases, respectively. A high value signal opens a gate-switch of a destination port, while low value signals keep close other switches.

2.3 Experiments

Figure 4 represents the experimental set-up of distributed OPS with two ports. Set-up consists of an optical packet transmitter and the OPS composed of label processor, 1×2 optical gate switch, and optical delay. An optical packet transmitter consists of 2 ps-10 GHz-MLLD, $LiNbO_3$ intensity modulators (IM), optical encoder, and optical delay. Optical encoder consists of tapped delay-lines with thermo-controlled optical phase shifters as shown in Fig. 4. All elements are monolithically integrated by using PLC technology. The optical carrier phase of each chip pulse is shifted either 0 or π by the phase shifter to generate the 8-chip BPSK-codes [11]. Label processor is comporsed of optical correlaters, photo detectors (PD), low-pass filters (LPF), and gate signal generator. The 1×2 optical gate switch consists of two IMs with 40 GHz bandwidth.

In the optical packet transmitter shown in Fig.4, IM 2 generates 64 bit-long packet data signal at 10 Gbit/s. IM 1 and optical encoder generate optical label which is 8-chip BPSK optical codes with a time interval of 5 ps. Generated optical code and payload data signal are combined to form a packet. In the label processor, if the input code matches with the code of a correlater, the output (correlated signal) takes a high value. On the other hand, in unmatched case, the correlated signal takes

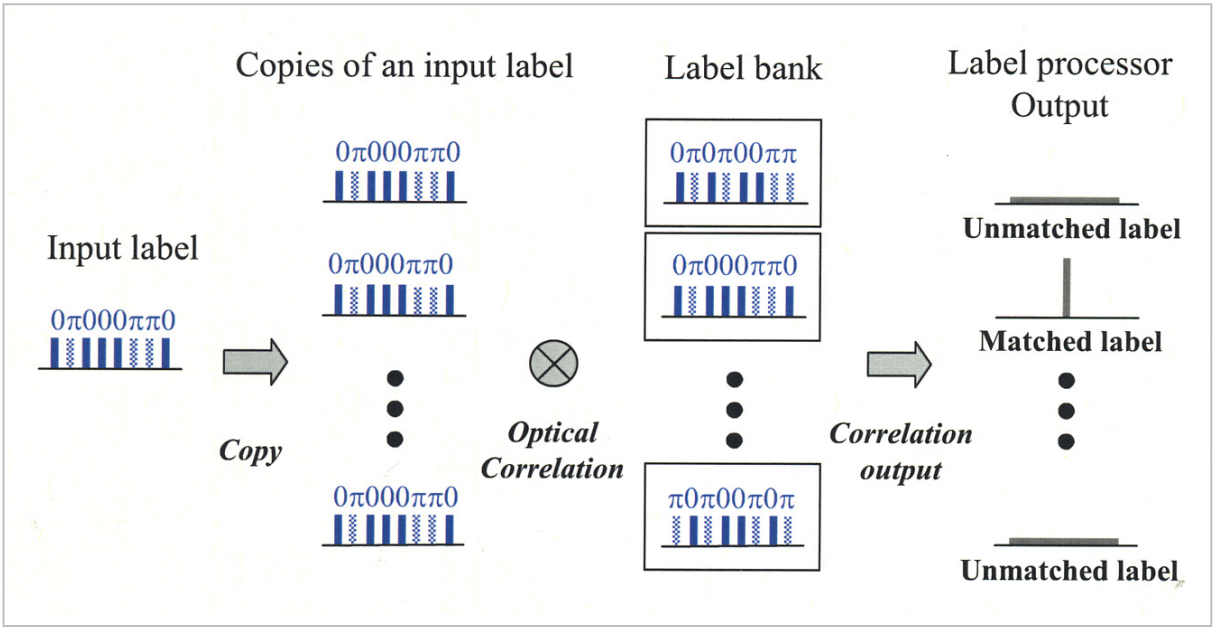

Fig.3 *All-optical parallel table look-up*

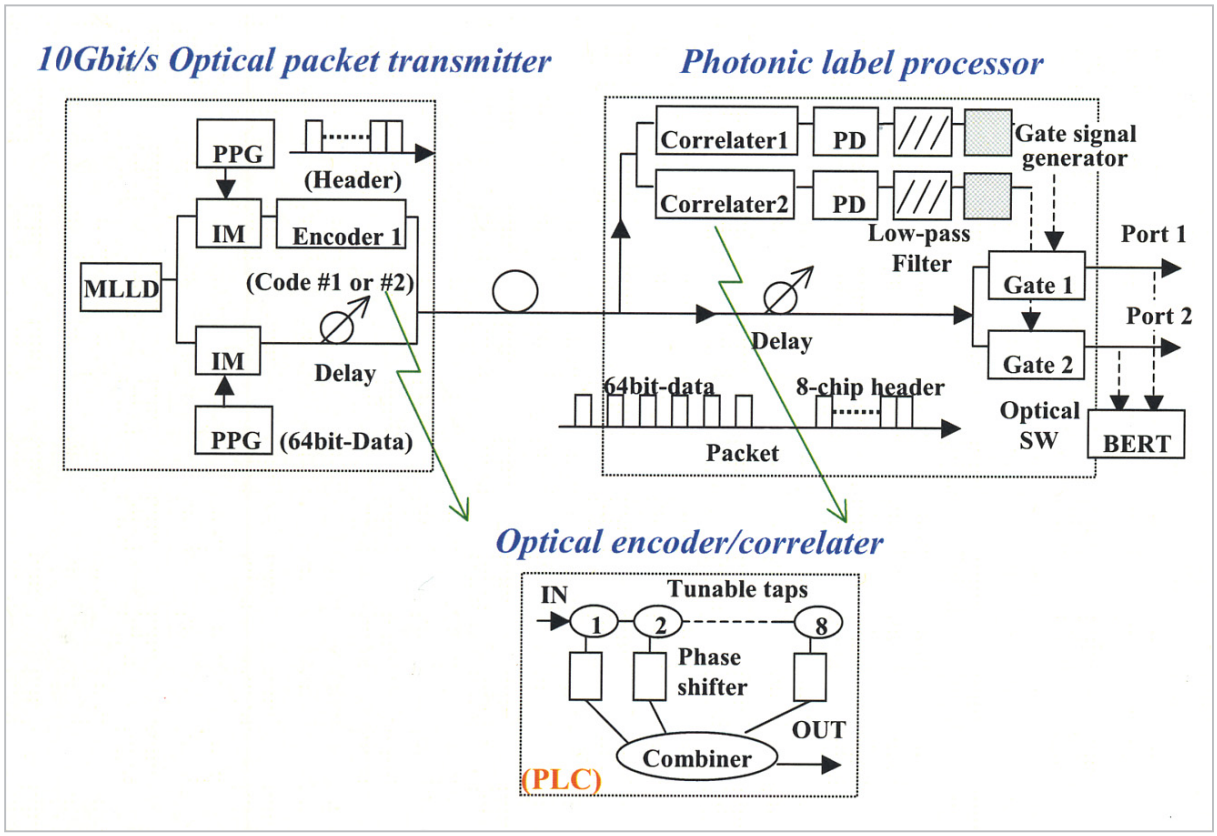

Fig.4 *Experimental setup*

lower value. In matched case, the correlation signal is converted to the electrical signal and used to gate and hold open the IM gate switch via gate signal generator. While in the unmatched case, the bias is not changed, then the gate switch still close. The label processor can open an objective gate switch and routs the matched packet to the target port.

Figure 5 (a) is a streak camera trace of a generated packet with an optical code #1: "0π $\pi\pi\pi\pi\pi$0". Figure 5 (b) and (c) represent streak camera trace of correlater outputs to the packets with a header of code #1: "0$\pi\pi\pi\pi\pi\pi$ 0" (matched code) and a code #2: "0π0π0π0 π" (unmatched code), respectively. In both cases, each bit of payload data of the packet is spread in time domain by passing through the correlater and takes so small value in comparison with the decoded label that it does not operate mistakenly with gate switch.

Figure 6 (a) and (b) represent the measured payload data of Port 1 and Port 2 to the two different input packet having label of "0π $\pi\pi\pi\pi\pi$0" matched with correlater 1 and "0π

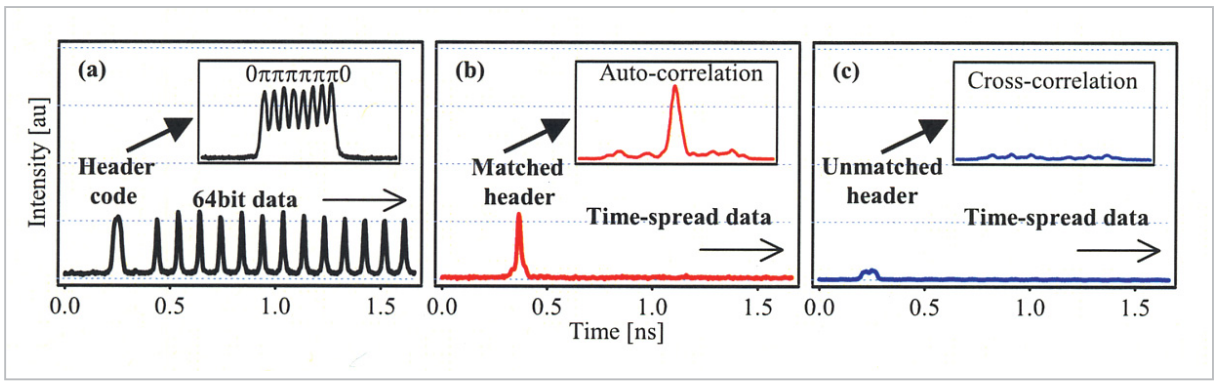

Fig.5 *Streak camera trace of (a) generated packet and correlated signals in (b) matched and (c) unmatched cases*

$0\pi0\pi0\pi$" matched with correlater 2, respectively. These clearly show that the address processor alternatively switches two optical gate switches as the input optical code switches between #1 and #2. It means that the label processor distinguish the 8-chip long optical codes label at the header of packets and control the optical switch. Figure 7 (a) and (b) are measured bit error rates (BER) of routed 64bit-long payload data with code #1 and #2, respectively, in each corresponding port. The measured BERs are less than 10^{-10}, which confirms the proper packet routing operation. Thses results guarantee the high speed OPS network.

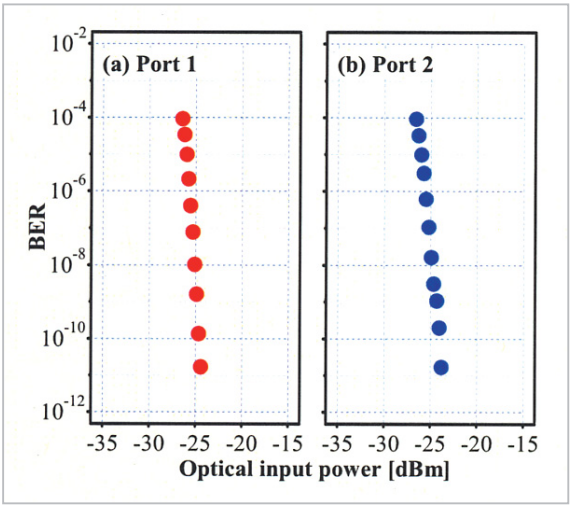

Fig.7 *Measured BER at (a) Port 1 and (b) Port 2*

3 Multi-wavelength label processing and variable length packet switching

3.1 Network architecture and packet format

We introduce a novel packet format consisting of a header, a payload, and a trailer in Fig.8 (a). The header has a label of a destination node. The label is K chip-long, each of which is one of W wavelengths. Figure 8 (a) represents a case of K=W=4. Here, λ_{1A}, λ_{1B}, λ_{1C}, and λ_{1D} are used to generate multi-wavelength labels. Variable length payload data uses different wavelength, λ_{1E}, from those used for label. The trailer is the same as the header. Wavelengths λ_{1A} through λ_{1E} make a wavelength band $\lambda_{1A\text{-}E}$. In each band, the same number of independent labels are generated and used as a header and a trailer of packet.

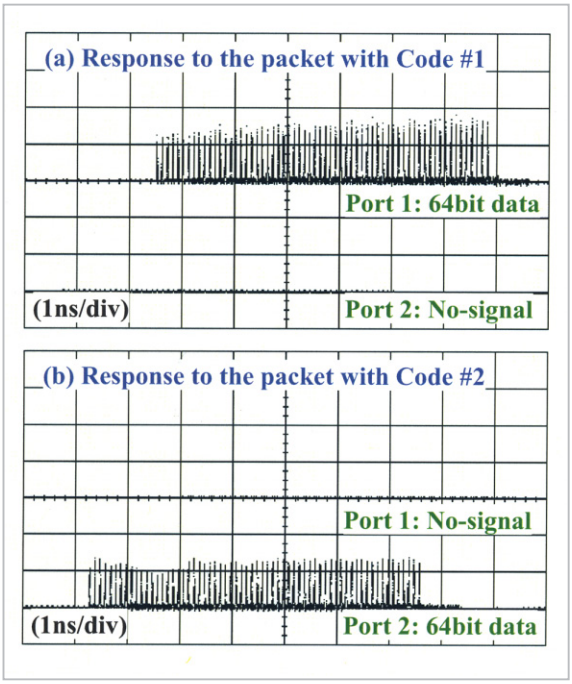

Fig.6 *Routed packet data with code (a) #1 and (b) #2*

Figure 8 (b) depicts the network architecture. It consists of multi-wavelength edge node (Mλ-EN), multi-wavelength label switching node (Mλ-LSN), and wavelength based optical cross connect (λ-OXC). Mλ-EN gives multiple wavelengths as a label. Mλ-LSN recognizes the multi-wavelength label in optical domain, and routes the packet to assigned port. Generation and recognition of multi-wavelength label are performed all-optically by multi-section fiber Bragg gratings (MS-FBGs). λ-OXCs switch the band. (See [4] in detail.)

A network with the Mλ-LSNs recognizes more optical label than a λ-LSN network. The label composition gives $W!/(W\text{-}K)!$ different labels to packets while the number of wavelengths is W. This means that $W!/(W\text{-}K)!$ Mλ-ENs can communicate with each other all-optically while W in the λ-LSN case. For example, assume that 16 wavelengths are given to the multi-wavelength label composition. The number of labels of a network with Mλ-LSNs is more than 4 billion, which

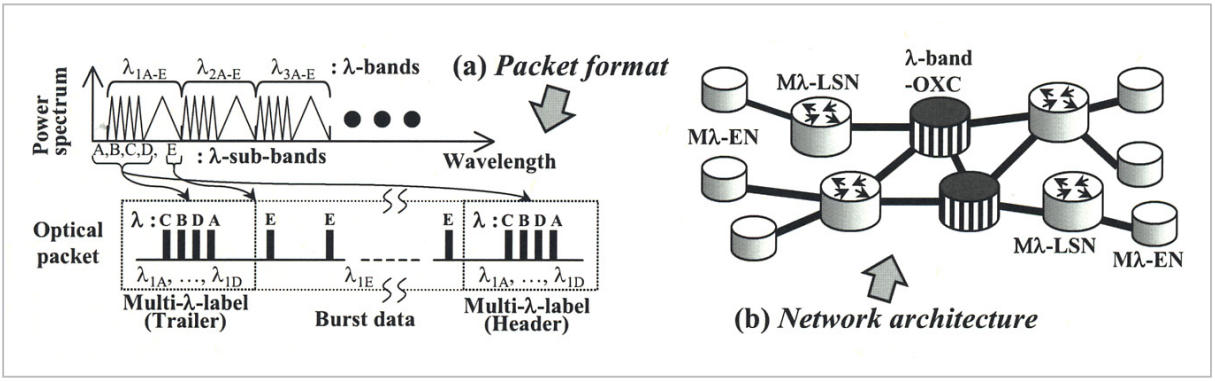

Fig.8 *(a) Packet format and (b) network architecture*

exceeds that of the Internet (2^{32}). Also, seven-wavelength label composition provides more than 6,000 labels, which is larger than the number of wavelengths in a future WDM technology.

3.2 Multi-wavelength label switch node

The block diagram of proposed Mλ-LSN is represented in Fig.9. The system consists of label and data separator, Mλ-label processor, switch (SW) controller, 1×N optical SW, output buffer and label swapper. Packet labels and payload data are separated by the separator. All optical label recognition and comparison with the label bank are performed in parallel manner by Mλ-label processor. Mλ-label processor outputs the open and close pulses at positions of packet header and trailer, respectively. SW controller controls the 1×N optical switch to transport the variable length packet to designated port via output buffer. If the packet need to swap its label, label swapper generates a suitable new label for the packet. In this experiment, output buffer and label swapper are omitted for simplicity.

3.3 Experiments

Figure 10 represents the experimental setup, which consists of Mλ-packet transmitter, 50 km dispersion-shifted fiber (DSF), and Mλ-LSN with 3 ports. An Mλ-packet transmitter consists of supercontinuum light source with bandwidth over 160nm (Fig.10(a)), $LiNbO_3$ intensity modulators (IM), 3 section FBG, band-pass filter (BPF), and optical delay. SC light source composed of 10 GHz Mode locked laser diode (MLLD), EDFA, and dispersion-flattened fiber (DFF) [4]. Mλ-pulse from SC source divides into 3 pulses by 3 section FBG to form the Mλ-label ("$\lambda_{1A}, \lambda_{1C}, \lambda_{1B}$" in Fig.10(b)). On the other hand pulse with wavelength λ_{1E} extracted by BPF, and variable length packet data is generated. Optical packet with 3-chip Mλ-label header and trailer and data are all-optically generated.

Mλ-LSN consists of FBGs (Figs.10(c)-(e)), photo detectors (PD), gate signal generator (SW controller), BPF, and delay. The 1×3 optical gate switch consists of three IMs with 40 GHz bandwidth. The gate signal generator composed of thresholder, limiting RF amplifi-

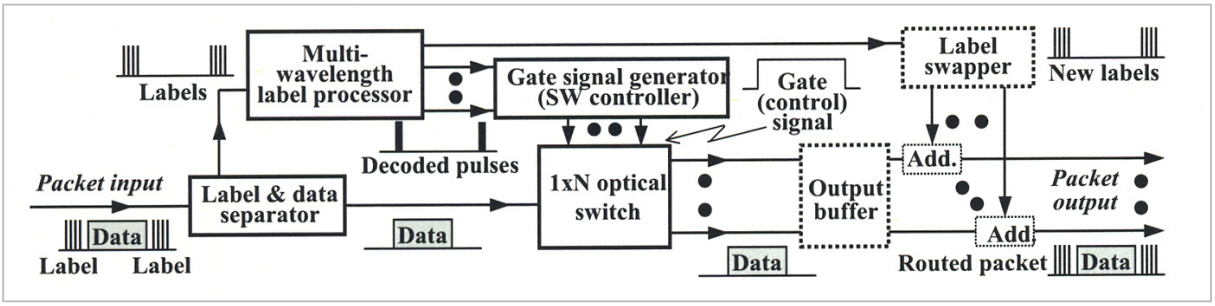

Fig.9 *Multi-wavelength label switch node for variable length packet*

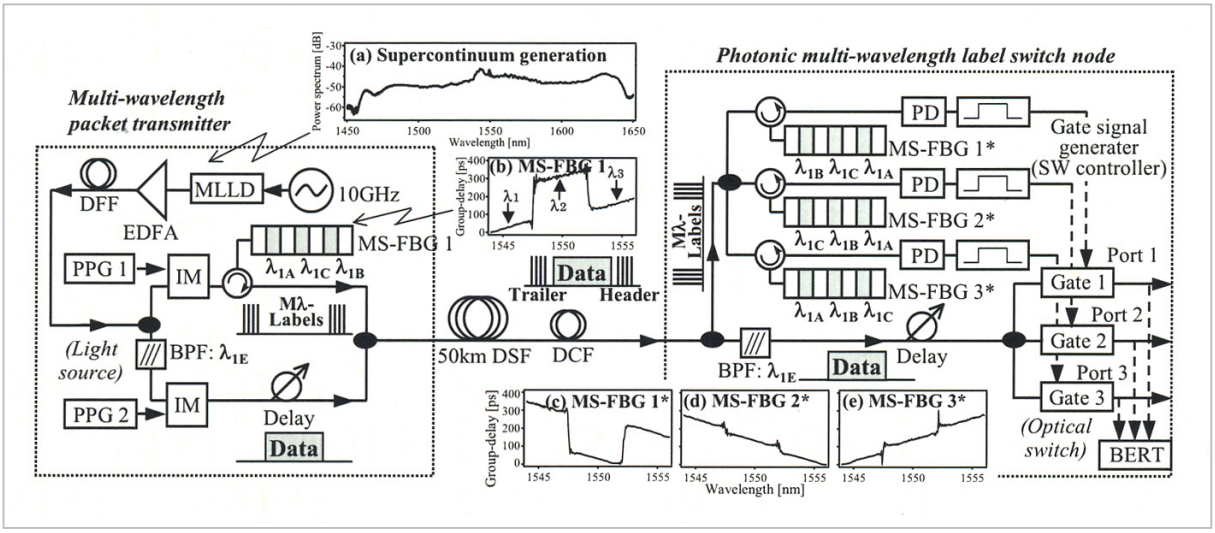

Fig.10 *Experimental setup*

er, and T-flip-flop. In the Mλ-LSN, FBGs play the role in correlater and label bank. If the input label is matched with the λ set of a correlater, the output takes a high value. Otherwise, the correlated signal takes lower value. The correlation signals are converted to the electrical pulse signals by PD. In matched case, a pulse at matched header label open the IM gate switch, and a pulse at matched trailer label close the switch. While in the unmatched case, the bias is not changed, then the gate switch keeps close. The label processor can open an objective gate switch and lead the matched variable length packet to the designated port.

Figure 11(a) is the generated 64bit long packet with header and trailer of Mλ-label: "$\lambda_{1A}, \lambda_{1C}, \lambda_{1B}$". Figure 11(b) and (c) represent correlation outputs of FBG1* with a λ set "λ_{1B}, $\lambda_{1C}, \lambda_{1A}$" and FBG2* with a λ set "$\lambda_{1C}, \lambda_{1B}, \lambda_{1A}$" to the input label "$\lambda_{1A}, \lambda_{1C}, \lambda_{1B}$", respectively. In matched case (Fig.11(b)) correlation signal has a high peak, while unmatched case (Fig.11(c)), the signal has no high peak. This is a demonstration of the all-optical Mλ-label recognition. Figure 11(d)-(f) represent the switched payload data at Ports 1, 2, and 3 to the three different length input packets; (d) 64 bit data with label "$\lambda_{1A}, \lambda_{1C}, \lambda_{1B}$" matched with FBG1*, (e) 128 bit data with label "λ_{1C}, $\lambda_{1B}, \lambda_{1A}$" matched with FBG3*, and (f) 192 bit data with label "$\lambda_{1A}, \lambda_{1B}, \lambda_{1C}$" matched with FBG2*, respectively. These clearly show that the Mλ-LSN can switch variable length packet, which depends on the input optical label. Figure 11(g) is measured BER at Port 1 in cases of back-to-back and after 50 km transmission of three different length packet. These results guarantee the ultra-high speed OPS network using multi-wavelength label processing.

4 Holographic label processing by AMSH

The angular multiplexing capability of holograms has been shown for implementing large-scale parallel optical storage. We expect to reduce the number of correlator in an optical label processor by using an angular-multiplexed spectral hologram (AMSH) as an address bank [9]. The holographic label processor is shown in Fig.12 (a). The holographic label processor is composed of diffraction grating, Fourier transformation lens and AMSH. The label with destination address information separates time and spatial axis by the diffraction grating. This diffracted signal passes through the Fourier transformation lens and is incident on the spectral hologram as objective light. Some labels have been recorded in angle-multiplexed manner. The reconstructive light, which is produced by an AMSH, passes through the Fourier trans-

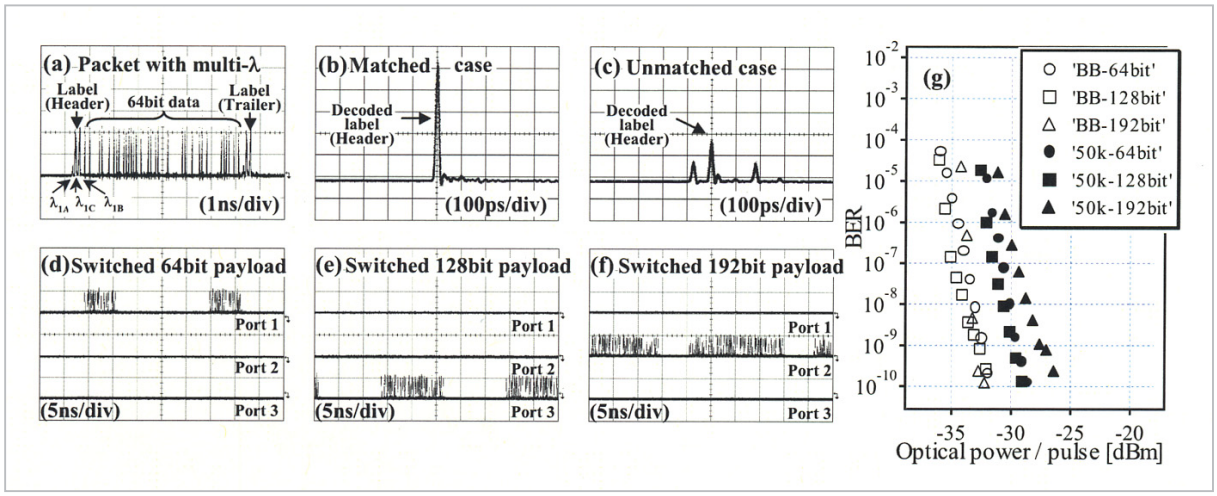

Fig.11 *Experimental results*

formation lens again and outputs as a correlation peak to the position depending upon the each incidence label (see Fig. 12 (b) and (c)). The light detected by PD array. Address information in each label is detected as the position information on the PD array. The signal activates the optical gate switch to route the optical data packet to the designated port.

In the spatial label recognition, it is necessary to use the spatial patterns of signals. Several groups have reported all-optical time-to-space conversion techniques that entirely separate the temporal and spatial axis. However, in our system, it is necessary not the complete

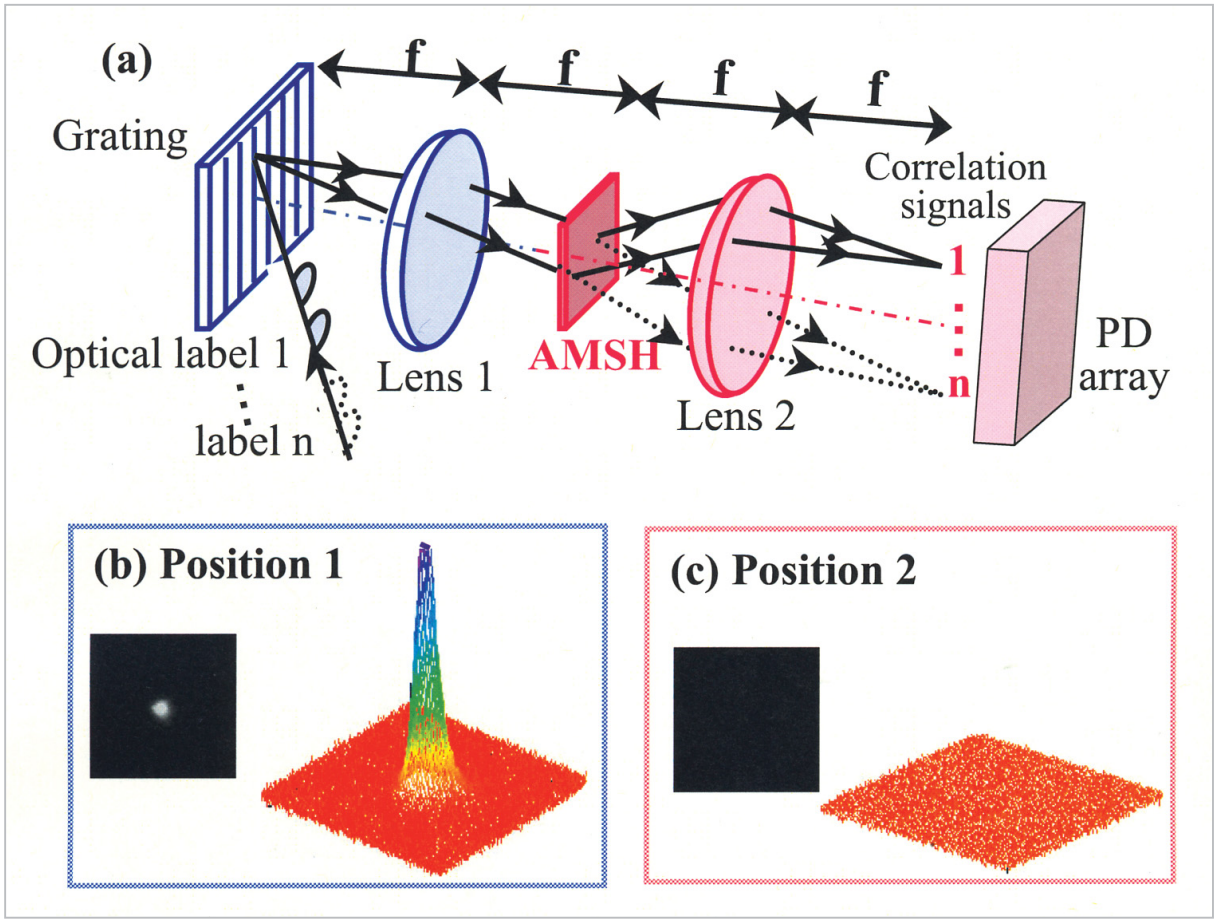

Fig.12 *(a) Holographic label processor and measured intensity distribution at (b) Position 1 and (c) Position 2*

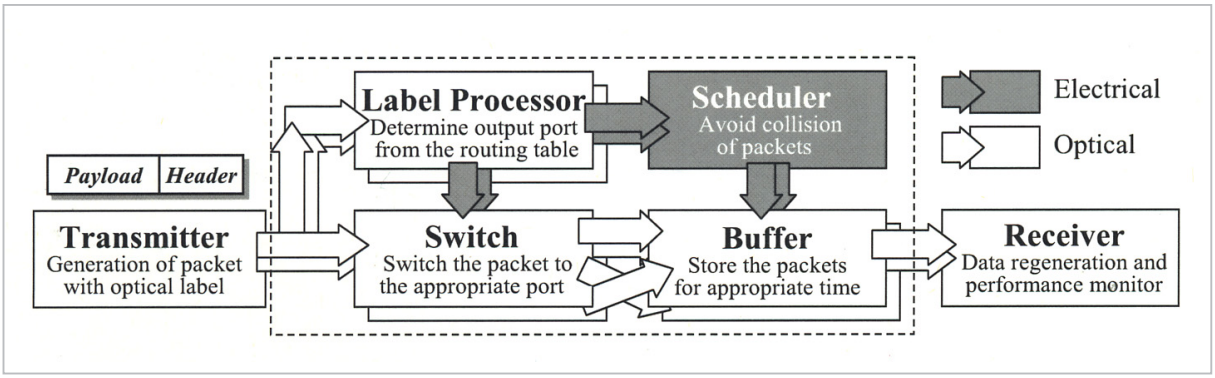

Fig. 13 *Block diagram of the prototype*

Table 1 *Specifications of OPS prototype*

Architecture	Optical packet switch with output optical buffer	
Input ports	2	
Output ports	2	1 (in experiment)
Buffer size (maximum delay)	2 packets (1024ns)	
Maximum data rate	39.81312 Gbit/s (correspond to OC-768)	
Label recognition speed	10 billion packets/s/port	<100ps / packet
Label recognition method	Optical matched filtering by using PLC based correlator and 8-chip BPSK codes	Asynchronous
Optical switch	A set of 1x2 switches	Coupler with LiNbO3 gate switches
Scheduling	Round robin, FIFO	For synchronous packets (T=512ns)
Buffer architecture	A series of 1x2 $LiNbO_3$ switches	Overflowed packets are rejected

time-to-space conversion pattern, but spatial patterns reflect the temporal waveform of the signal [10]. The individual frequency components contained within the incident signals are angularly dispersed by the diffraction grating, and then focused at the back focal plane of the lens, where the frequency components are spatially separated along one dimension. Therefore, we produce the AMSH by using spatially dispersed optical Fourier components. This label processing method is expressed in detail in a recent report [12].

5 40 Gbit/s interface OPS prototype

5.1 Prototype architecture

Recently, we have developed 40 Gbit/s interface, all-optical code-label processing based OPS prototype [8]. Figure 13 represents the block diagram of the prototype. The prototype consists of optical label processor, optical switche, electronic scheduler, and optical buffer. As parts of the prototype, we also developed optical packet transmitter with OTDM multiplexer and optical packet receiver with OTDM de-multiplexer for the performance analysis. An optical packet consists of a header and a payload data as shown in Fig. 13. The header has an optical code-label representing a destination node. In the label processor, a packet header label is analyzed all optically.

5.2 Label processing and switching

In our OPS prototype, we introduce label recognition method (a) in Fig.1. Label processor controls the optical switch and gives packet arriving information to the buffer scheduler. By separating the individual functions of a packet switch, we can fully use all-optical label processing capability. The specification of the prototype is represented in Table 1. The prototype is a 2×2 packet switch. We assume that packets arrive synchronously in order to simplify buffer architecture. The packet length is fixed. The inter-arrival time of the packets at each port is a multiple of T, where T is the time equivalent to the sum of the packet length and guard time.

The optical packet transmitter generates 8-chip, 200 Gchip/s optical BPSK label and 40 Gbit/s, 16000 bit random burst data to form an optical packet. The waveform of generated optical packets is shown in Fig. 14(a). The label processor consists of PLC correlators and optical switch driver. Table lookup of the packet label is performed in a parallel manner without O/E and E/O conversions [3] as described in Section 2. In case of matched label, the correlator outputs the autocorrelation waveform with high peak (Fig. 14(b)) and opens the target optical gate switch to routes the packet to destination port. In case of

unmatched label, the correlator outputs cross-correlation waveform without high peak (Fig. 14(b)) and keeps close the gate. The scheduler supports synchronously arriving fixed-length packets. It receives packet arrival information from optical label processors. It handles the information first-in-first-out (FIFO) basis and according to round robin scheduling. Optical switch consists of coupler and SOA gate switches. Waveforms of switched packets from two different input ports to the same output port are shown in Fig. 14(c). The prototype has output buffers. We develop a fiber delay line (FDL) buffer in which the sum of the lengths of FDLs is different dependent on a physical route [13]. Moreover, It is necessary that appropriate FDLs be selected for each arriving packet before it arrives at the FDL buffer. In order to avoid packet collision and decrease packet delay, we develop a field programmable gate array (FPGA) based electronic scheduler, which counts the number of packets in the buffer and provides control signals to optical switches in the buffer. Waveforms of buffered packets from two different ports are shown in Fig. 14(d). Finally, these buffered packets are merged and output to a port. The output packets waveforms are shown in Fig. 14(e). Measured BERs at back-to-back, output of SOA switch, and outputs of a buffer are represented in Fig. 14(f). These results guarantee the 40 Gbit/s photonic packet switching. The results are expressed in Ref [15] in detail.

6 Conclusion

Ultra-high speed all-optical label processing methods have been proposed and experimentally demonstrated. These methods dra-

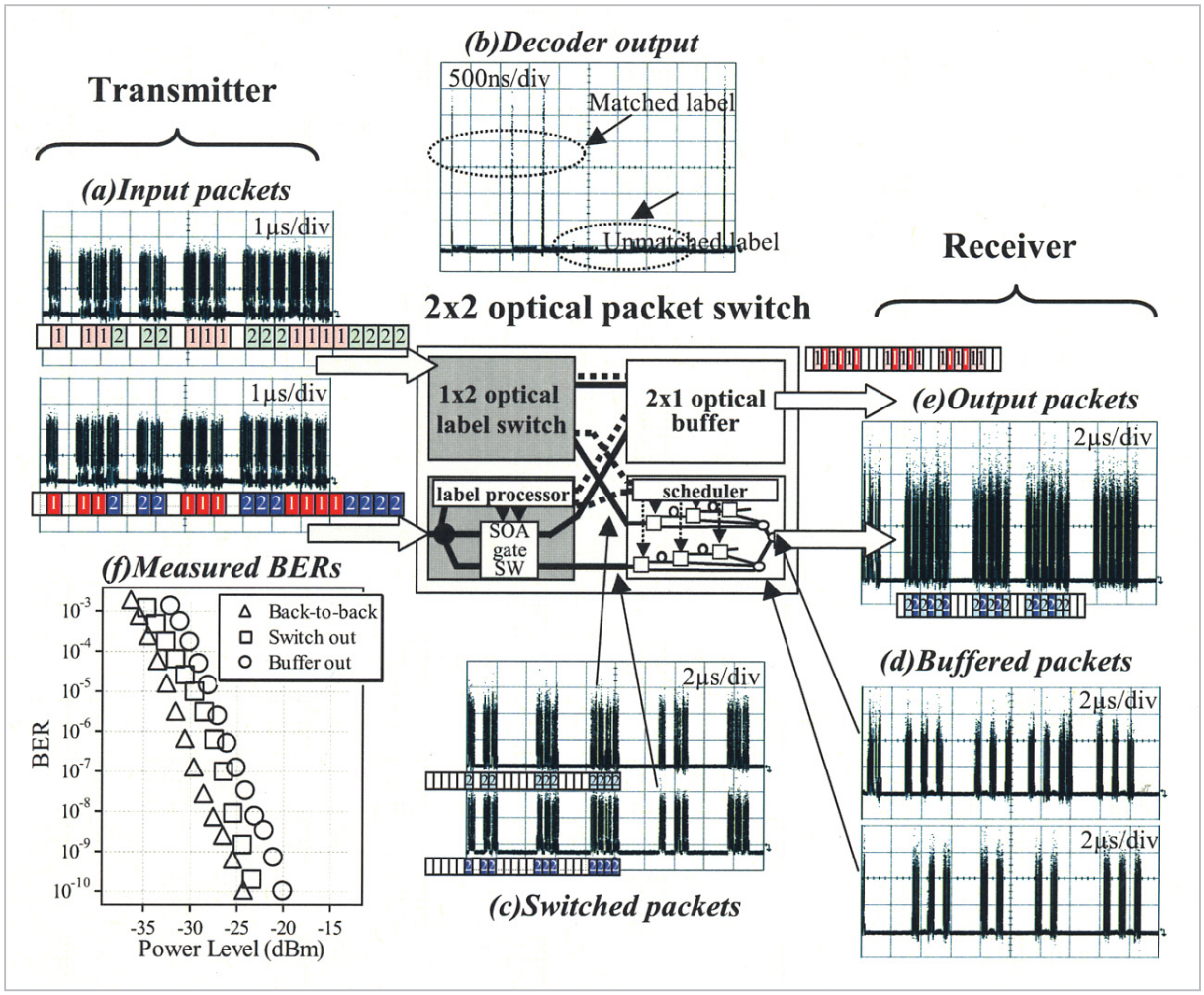

Fig. 14 *Experimental demonstration of OPS prototype*

matically have increased the label processing capability. Optical packet switch (OPS) systems and networks based on OPS nodes have been expressed as an application of optical processing technologies. First 40 Gbit/s/port OPS prototype with all-optical label processor, optical switch, optical buffer, and electronic scheduler has been expressed. The feasibility of OPS networks has been verified by experimental demonstrations.

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