4-6 Design Infrastructure of Large-scale Single-flux-quantum Logic Circuit

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Single-flux-quantum (SFQ) circuit is a quantum effect device operating by controlling the wave nature of electron. The energy required for the control of SFQ motion is quite low, which enables high-speed logic operation with low power consumption. We have constructed design environment of the large-scale SFQ circuit to apply high-end router in the backbone network. We have so far succeeded to demonstrate the perfect operation of the network switch circuit consisting of more than 5000 Josephson junctions at 30 GHz, showing the availability of our design methodology of large-scale SFQ circuits.

Keywords
Single-flux-quantum, Integrated circuit, Josephson junction, Network device, Cell-base design

1 Introduction

Semiconductor integrated circuit technology is unmistakably the key technology supporting today's advanced information society. Operating clock frequency has already exceeded 3 GHz, and density has reached 100 million transistors per chip. The evolution of semiconductor integrated circuit technology has been supported by the so-called scaling law applied to CMOS (complementary metal-oxide semiconductor) circuits. The scaling law states that if the size of a device is reduced to 1/k, density improves by k^2, power consumption improves by $1/k^2$, and delay is improved by 1/k [1]. However, this scaling law has recently begun to reveal its limitations [2]. These are not simple technical limitations involved in reducing device size, but instead are related to the nature of device operation, such as the appearance of quantum effects associated with miniaturization. Single-flux-quantum (SFQ) logic circuits are quantum-effect devices that operate based on a completely new principle of operation, offering a potential means of overcoming the limitations of semiconductor integrated circuits.

2 Principle of operation of SFQ circuits

Figure 1 shows a schematic diagram of the principle of operation of SFQ circuits. An SFQ circuit operates through application of the phenomenon in which magnetic flux is quantized on entering a superconductor loop. A device known as a Josephson junction is built into the loop to control the motion of SFQs into and out of the loop. The Josephson junction makes use of the tunnel phenomenon seen in superconducting electron pairs. The device can be regarded as a switch that turns on and off at high speed. In Fig. 1, if the Josephson junction on the left is off (it is on in the stationary state) while there is no SFQ in the loop, an SFQ enters the loop, changing the state to "1". If the Josephson junction on the right is off, the SFQ maintained in the loop moves out of the loop, changing the state back to "0" with no SFQ. Any digital operation

becomes possible using SFQs as information carriers and combining superconducting loops [3].

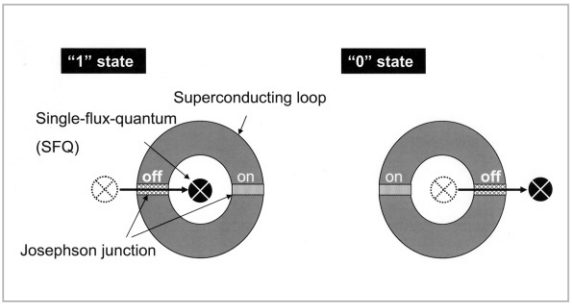

Fig.1 *Operation principle of an SFQ circuit*

Why is magnetic flux quantized in a superconducting loop? The answer to this question is closely related to the wave nature of electrons. As electrons behave as waves in a superconductor, the phase of an electron is always a multiple of 2π as it circuits the loop for the first time. The state in which an SFQ is contained within the loop corresponds to the state in which an electron with a phase of 2π is carried within the loop. In other words, the SFQ and the phase of the electron are in one-to-one correspondence, and an SFQ circuit can thus be regarded as a quantum-effect device operating to control the phase of the electrons. The essential difference between an SFQ circuit and a semiconductor integrated circuit such as a CMOS is in that an SFQ circuit makes active use of the wave nature of electrons, whereas a semiconductor integrated circuit operates by controlling the particle nature of electrons.

3 Performance comparison between electronic devices

3.1 Power-delay product (energy)

Applying quantum effects will not necessarily guarantee better performance in electronic devices. Yet what determines the superiority of an electronic device? An electronic device that operates more rapidly (i.e., with little delay) and with less power may be considered a better electronic device. This means that the energy value corresponding to the product of power and delay should be small. Power consumption aside, many semiconductor devices operate at high speeds. For example, bi-polar transistors and HEMTs (High Electron Mobility Transistors) have long been known to operate at high speeds. Nevertheless, the CMOS is by far the most popular digital computing device, due to its low power consumption. Thus the SFQ circuit must offer a lower power-delay product (i.e., lower energy) than CMOS to survive as a digital computing device.

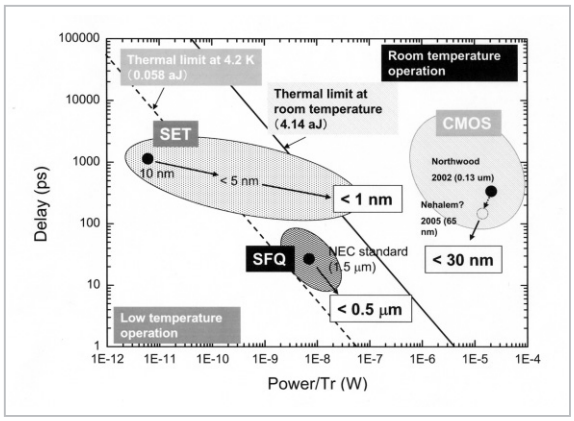

Fig.2 *Power-delay map*

Figure 2 shows a power-delay map of various devices, with the delay of the device on the vertical axis and the power consumption per transistor (per Josephson junction) on the horizontal axis. This map plots the approximate positions of low-power devices, including the SFQ circuits. In Fig. 2, the energy (power-delay product) is constant along the diagonal line from the top left to the bottom right. As discussed above, the lower the energy, the better the performance. However, stable logical operation (without error) requires a level of energy sufficiently exceeding thermal noise (k_BT: k_B is the Boltzmann constant, T is the operation temperature). In Fig. 2, CMOS circuits fall distinctly to the right of the thermal noise limit line at room temperature (represented by the red line). On the other hand, the single electron transistor (SET), operating with a single electron [4] [5], is currently positioned to the left of the thermal noise limit at 4.2 K (blue line), which means that it operates

only in extremely low-temperature environments. SFQ circuits fall generally midway between these two types of devices on the power-delay map. A problem arises, however, when we consider future development. CMOS devices offer reduced delay and power consumption in accordance with the scaling law, but it is unclear to what extent these devices will be able to approach the thermal noise limit now that the scaling law has begun to reveal its limitations. On the other hand, the SET is designed with an eye to the opposite direction, in an attempt to cross to the right of the thermal noise limit. Although it is assumed that the device will be operable at room temperature if it can be fabricated on the sub-nanometer scale, many problems must first be overcome [6]. Given the foregoing, it is evident that the SFQ circuit's position on the power-delay map renders this device extremely attractive. Although the operating temperature is 4.2 K, this device is already located near the thermal noise limit, which the CMOS and the SET are aiming to reach.

3.2 Operating speed

Operating speed alone cannot be used to evaluate the performance of a digital computing device, but it does provide one measure of performance. The operating speed of a CMOS circuit is determined by the charge and discharge time. As shown in Fig. 3 a), this device can be understood with an analogy to water accumulating in a channel between two gates. Here, the charge and discharge time is given by the product of the capacitance and the resistance of the device (the CR time constant). This is several hundred picoseconds in the 130 nanometer technology node. If the channel is shortened, or if the mobility of the channel material is increased, the CR time constant can be reduced further. However, now that the scaling law is beginning to break down due to the appearance of quantum effects, including an increase in tunnel current (leak current), it is of particular interest to examine how far the CR time constant can be reduced in the future while avoiding increasing power consumption (particularly the power consumed when the device is off) [7].

On the other hand, a SET is a quantum-effect device that makes use of the electron tunnel phenomenon. However, its mechanism is the same as that of the CMOS in the respect that delay is determined by the charge and discharge time. It is different from the CMOS in that it operates based on the charge and discharge of a single electron (in the water analogy, this would correspond to a single drop of water). It should be noted that SET devices feature high impedance and that this characteristic renders the CR time constant generally large. In the analogy illustrated in Fig. 3 a), the SET makes use of a water drop that does

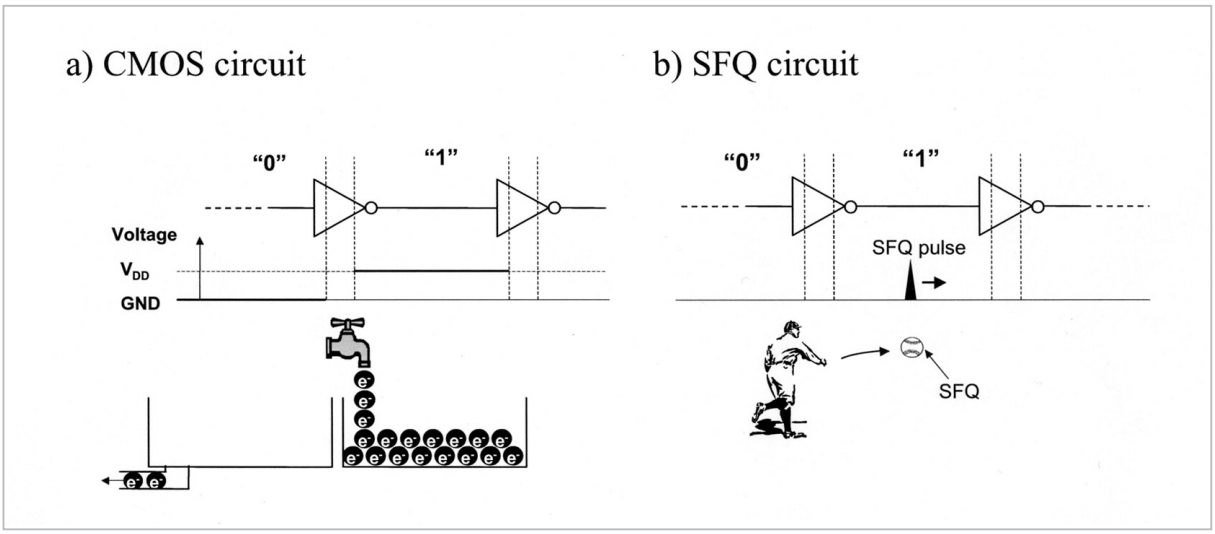

Fig.3 *Comparison of CMOS circuit operation and SFQ circuit operation*

not readily fall from the tap.

Unlike the CMOS or the SET, the operating speed of an SFQ circuit does not depend on charge or discharge. As shown in Fig. 3 b), an SFQ moves like a ball between the gates in an SFQ circuit. When an SFQ moves, it is always accompanied by a voltage signal (a voltage pulse at intervals of several picoseconds) the time integral of which produces the SFQ. This type of ballistic signal transport is similar to that observed in optical devices, and the SFQ moves within the chip at approximately the speed of light. In other words, an SFQ circuit is an electronic device that combines the high speed of an optical device with the high functionality of a semiconductor device.

To discuss the operating speed of an SFQ circuit more precisely, the delay within gates should be considered as well as the delay between gates. The delay within a gate depends on the switching time of the Josephson junctions and is in principle smaller with a smaller junction area. Currently under the so-called NEC standard process [8], which specifies processing techniques to ensure a minimum fabrication size of approximately 2.0 μm, the switching time of a Josephson junction is approximately 3–4 ps. There are three or four switching Josephson junctions within a logical gate from input to output, resulting in total delay of 9–16 ps. This delay, added to the delay between the gates, determines the operating speed. Operating speed today is limited to approximately 50 GHz (corresponding to a delay of 20 ps). However, refining the Josephson area to the submicron region will be sufficient to provide operating speeds of over 100 GHz.

4 Application of SFQ circuits and future problems

When considering the applications of an SFQ circuit, it must be considered that the relevant operation temperature will be extremely low (4.2 K). In other words, an SFQ circuit always requires a refrigerator, rendering it unsuitable for general-purpose applications. Following is a list of some examples of applications proposed or studied to date.

(1) High-end equipment (routers, servers, computing, etc.)
(2) AD (analog/digital) converters
(3) Quantum bit control circuits
(4) Signal-processing circuits for various superconducting sensors

Regarding the applications covered under item 1 in the above list, the cost of power consumption for routers in backbone networks exceeding 10 Tbps is estimated to correspond to several hundred million yen; if SFQ circuit technology were to be introduced, equivalent performance might be achieved with power consumption of 1% the current amount or less, including cooling. Related research has been conducted on network devices such as routers and servers in Japan [9] [10], and on high-end computing devices in the U.S. [11] [12]. Applications indicated in item 2 are also under intensive study worldwide, involving mainly high-performance AD converters for software radio base stations [13] [14]. As for item 3, it has been demonstrated that quantum bits can in fact be realized using SFQs. These applications include attempts to control quantum bits with SFQ circuits. The applications indicated in item 4 currently represent the most realistic use of SFQ circuits today, as the only limiting condition is found in the required use of refrigerators in the relevant sensor sections.

These applications vary greatly, but all require a scale of integration involving twenty thousand Josephson junctions or more, representing the upper limit of integration on a 5×5 mm^2 chip given current processing techniques. The design of such a large-scale SFQ circuit represents a significant outstanding problem. Although analog semiconductor devices have already been designed to operate in frequency bands at or above 10 GHz, an extremely significant challenge remains in the design of a large-scale digital circuit that can operate at or above several tens of gigahertz.

5 Large-scale SFQ circuit design through the cell-base method

The cell-base method has been introduced for large-scale efficient design of an SFQ circuit. The cell-base method enables circuit design using a cell library in which information regarding each logic gate is registered separately, including operation data, delay information, and mask layout. This method is commonly used in semiconductor circuit design but requires modification when applied to SFQ circuits, as the relevant principles of operation are different. Figure 4 shows the structure of the SFQ cell library we have developed and shows the corresponding design flow. This SFQ cell library was developed with the collaboration of the National Institute of Information and Communications Technology (NICT), the NEC Fundamental Research Laboratories, Nagoya University, and Yokohama National University. This library was given the acronym CONNECT (Cooperation of Nagoya Univ., NEC, CRL and Yokohama National Univ. Team)Cell Library [15].

The design makes use of the CAD (Computer Aided Design) tool environment provided by CADENCE. The circuit is first assembled on the schematic editor through operations in what is referred to as the "Symbol View," in which the types and sizes of cells are identified. Each cell has various Views in addition to the Symbol View. For example, the so-called "Schematic" View mainly describes the most primitive equivalent circuit, consisting of Josephson junctions and inductances. It is possible to generate a net list of primitive circuits, including Josephson junctions, by simply arranging the Symbols in the schematic editor. However, simulation of these primitive circuits (referred to as analog simulation) takes an enormous amount of time, so an alternate method referred to as timing simulation is used to verify operation of large circuits. Timing simulation is performed based on the timing parameters extracted for each cell from analog simulations. The hardware description language referred to as Verilog-XL is used to describe the timing parameters. The ultimate goal of the cell-base method is to enable the circuit designer to

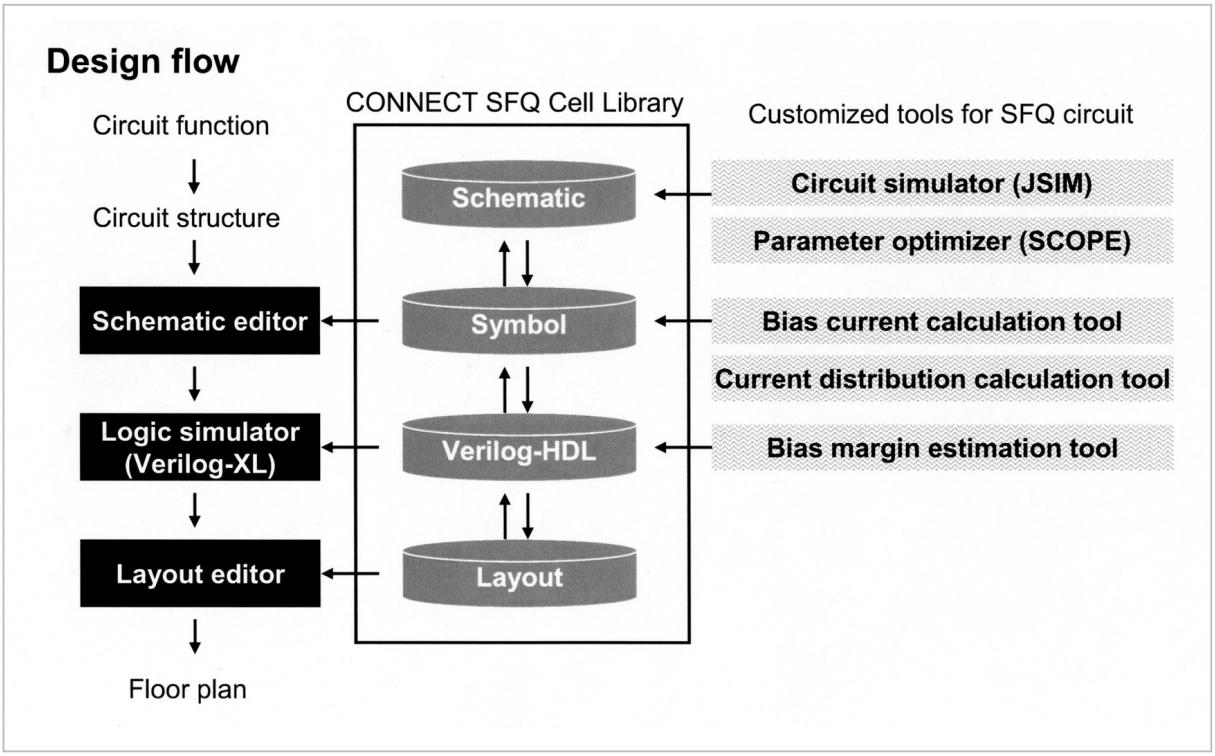

Fig.4 *Design flow of a large-scale SFQ circuit*

design an SFQ circuit without the need to take the SFQ nature of the circuit specifically into account.

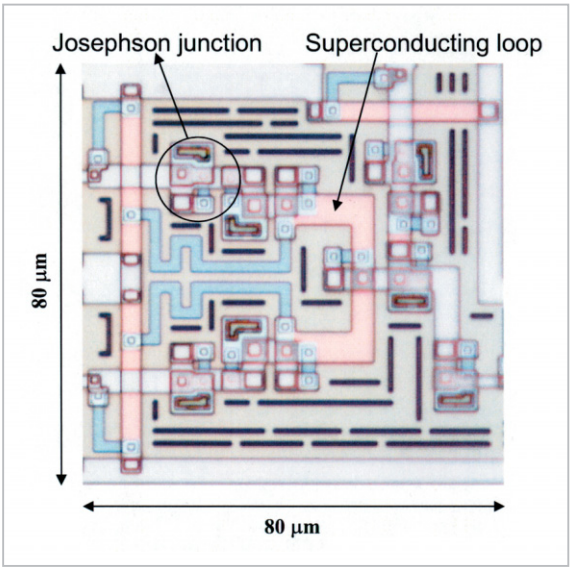

Fig.5 *Microphotograph of an SFQ cell*

A significant issue in cell-base design involves optimization of the parameters of primitive circuits (e.g., critical current and inductance of the Josephson junctions). We optimized the parameters with the SCOPE optimization tool developed by Nagoya University and succeeded in obtaining ±25% operation margins or more for all cells. Figure 5 shows a microphotograph of an SFQ cell (an Ex-OR gate). The cell is rectangular, with a normalized size of 40 μm. The positions of the signal input and output ports are determined in consideration of the connections with other cells. There are 11 Josephson junctions in this cell. Other logic cells also contain approximately 10 Josephson junctions.

6 Demonstration of the network switch circuit operation

Network traffic in backbone networks continues to increase with the spread of the Internet and the recent introduction of broadband communications. Although fiber optics and the Wavelength-Division Multiplexing transmission technique have made it possible to transmit vast amounts of information, devices requiring electrical processes (such as routers) may be the cause of bottlenecks in the realization of future high-capacity networks. We have positioned SFQ circuits as key components in the realization of such a high-capacity router for backbone networks and have been designing an SFQ network switch circuit with this in mind.

Figure 6 shows the tandem Banyan switch fabric used in this study [16] [17]. It features a simple configuration, consisting of Banyan networks that transmit packets to the desired output ports through self-routing, TMC circuits—which distribute the packets in two directions, depending on the flag information—and an output buffer. If two packets crash in a Banyan network, one of the packets is always transmitted to the wrong port. However, a flag is attached to this incorrectly transmitted packet upon collision to notify the system. The TMC checks for this flag and the correctly transmitted packets are transmitted to the output buffer while the remaining packets are transmitted to the next-stage Banyan network. Repeating this process several times allows all packets to be transmitted to the desired output port.

A Banyan network consists of what are referred to as 2×2 switches, each featuring two input and two output ports. As each 2×2 switch has an address decoder, it functions as a self-routing switch. The built-in address decoder increases the circuit size of each 2×2 switch, but it eliminates the need for a complicated circuit to control the entire switch system. This characteristic will facilitate improved scalability of the overall switch.

Figure 7 shows a block diagram of a circuit that operated successfully in this study, the circuit chip being fabricated based on NEC's Nb standard process [8]. The circuit consists of a 2×2 switch and two TMCs, and represents the minimum unit of a tandem Banyan switch fabric. This circuit features a high-speed (approximately 20 GHz to 40 GHz) clock generation circuit and shift registers for data storage on a single chip, ensuring high-speed operation. The circuit uses

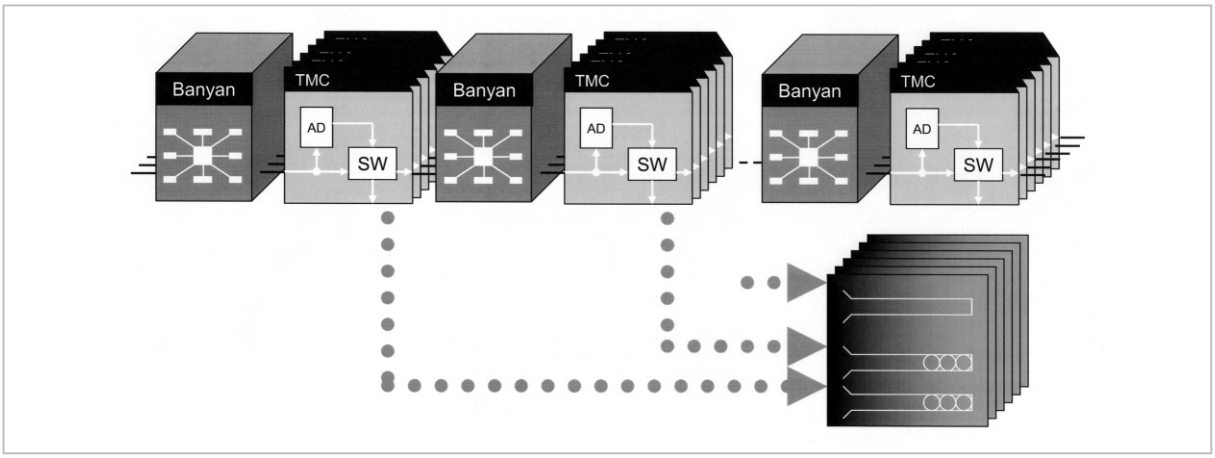

Fig.6 *Tandem Banyan switch fabric*

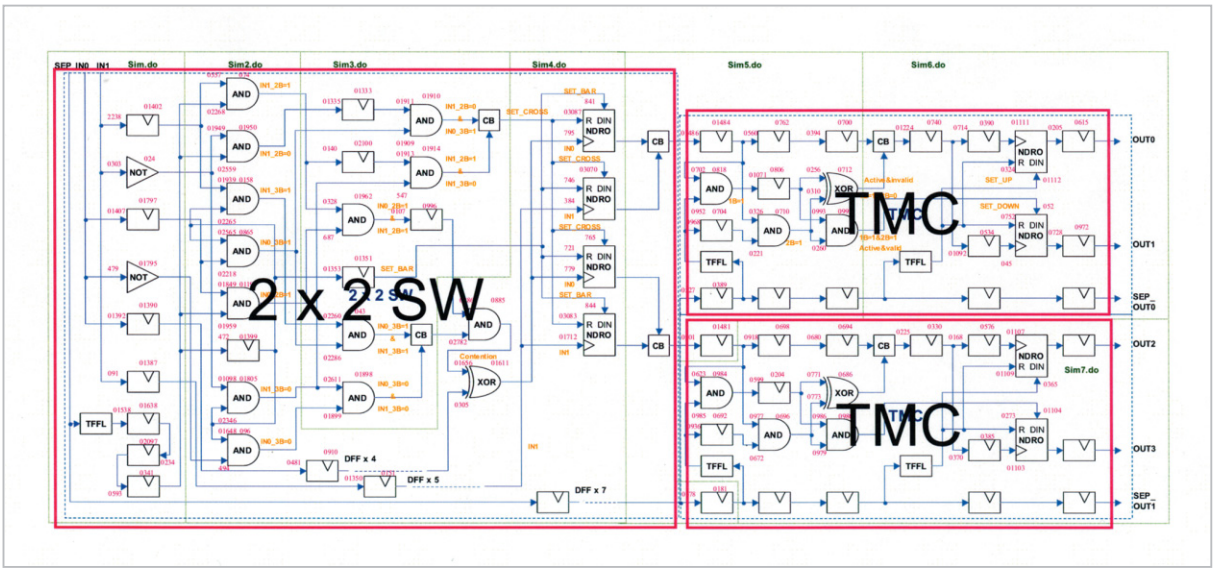

Fig.7 *Block diagram of the network switch circuit*

approximately 200 logic gates and 5,250 Josephson junctions.

This network switch circuit includes advanced functions such as control of crashed packets and priority packet control. The circuit is tested to ensure that all functions work correctly, and the results are used to confirm accurate operations for all test patterns. Figure 8 shows the operation-frequency dependence of the circuit in the normal region of operation. The area indicated in grey is the normal region of operation; the operating margin near the operation frequency of 20 GHz is approximately ±6%. As the frequency increases, the margin becomes smaller due to timing errors. Nevertheless, the switch was confirmed to operate correctly at 30 GHz.

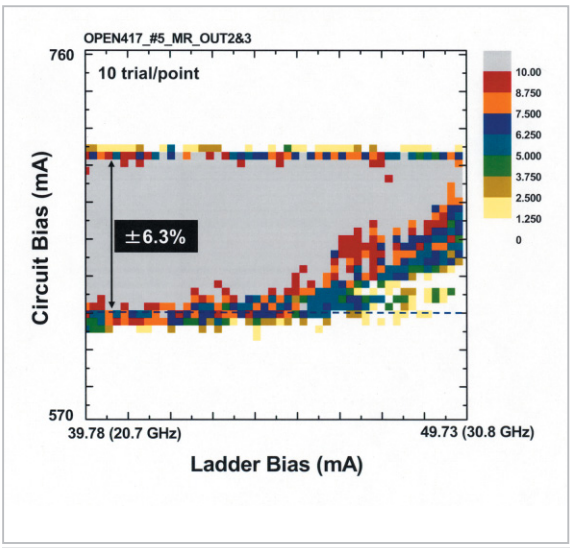

Fig.8 *Operating-speed dependence in the normal range of operation*

7 Conclusions

An SFQ circuit is a quantum-effect device that utilizes the wave nature of electrons, combining the functionality of a semiconductor device with the speed of an optical device. Various applications are anticipated, but the issue under study in this case was the demonstration operation of a large-scale circuit. Scientists and engineers from industrial, government, and academic organizations have collaborated in the development of an SFQ cell library and the cell-base design method. As a result, a network switch circuit containing 5,250 Josephson junctions has been shown to operate at a high speed of 30 GHz, confirming that the design method that we developed is effective in the design of a large-scale SFQ circuit. With the exception of CMOS devices, few circuits of this scale have been shown to operate in low-power devices. This experiment has confirmed that SFQ circuits represent potential candidates for post-CMOS devices.

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