Cryogenic Signal Processing Technology using Superconducting Single-Flux-Quantum Logic Circuit

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Superconducting single-flux-quantum (SFQ) logic circuit is an ultimate energy-efficient digital circuit technology. The SFQ circuits enable to enhance functionality and performance of various superconducting detectors by employing those as the cryogenic signal processors. We introduce the recent progress in the SFQ circuit technology focusing on the signal processing application combined with superconducting single-photon detectors (SSPDs).

1 Introduction

The nuclear power plant accident and the steep rise in oil prices have heightened the interest of the public in energy issues more keenly than before. Our surroundings are filled with various electronic and electric instruments. ICT devices such as personal computers, mobile phones and smart phones in particular deeply permeate our everyday lives and our social activities would no longer be feasible without them. Large-scale facilities such as routers of backbone networks and data centers, where information is concentrated, are also comprised in ICT devices. The annual rate of electric power consumed by the data centers in Japan, for example, is about to reach 10 billion kWh, which is equivalent to the amount of electric power generated by two nuclear power plants. There is a forecast that the rate of electric power consumed in 2020 by ICT devices, including terminal devices such as personal computers and smart phones, will account for 20% of the total electric power consumed in Japan. In addition to shifting to renewable energy, cutting back on power consumption by ICT devices has now become an urgent issue.

The brains of ICT devices are semiconductor integrated circuits, among which CMOS is the most typical. It is no exaggeration to say that the steady development of CMOS integrated circuit technology has built the ICT society. However, as the limitations of improvement in capability of the CMOS circuit have come to be recognized, significant increase in its performance would be difficult to attain. We have developed superconducting devices to achieve technological innovation in the field of information and communications. In this paper, the ultimate low energy logic circuit with a single flux quantum (SFQ) as an information carrier, its operating principle, characteristics and current developmental status are discussed. As its practical application, we will introduce its implementation as a signal processing circuit, integrated with a superconducting single-photon detector (SSPD) array, which we are currently developing.

2 Single Flux Quantum (SFQ) logic circuit

2.1 Operating principle

Today, information is processed mostly as digital information. Energy saving in digital information processing means that discrimination between "0" and "1" is carried out by using as little energy as possible. The amount of energy consumed at one switching (E_{SW}) by a single transistor in an advanced CMOS circuit is about 0.1 to1 fJ (femto-joule: 10^{-15} joules). An SFQ logic circuit that is incorporated with the property of superconductivity makes an action with an E_{SW} of 0.01 to 0.1 aJ (atto-joule: 10^{-18} joules), far smaller than the E_{SW} of a CMOS circuit. This value is equivalent to 200 to 2,000 times that of thermal noise at an operating temperature of 4K, suggesting great potentialities of the SFQ logic circuit as an ultimate low energy information processing technology.

The SFQ circuit uses magnetic flux (flux quantum: 2.07×10^{-15} T) quantized in a superconductivity loop as information carrier[1]. Figure 1 shows the operating principle of the SFQ circuit. Combinations of more than one superconducting loop and Josephson junction, which functions as a switch to take flux quantum in and out of a

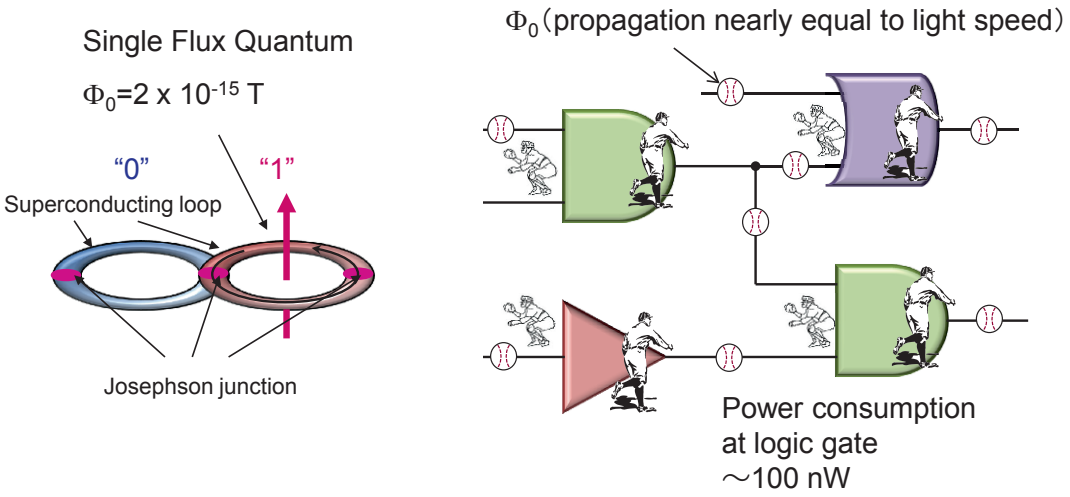

Fig. 1 Operation principle of SFQ circuit

loop, make various logical operations possible. Transactions taking place at a gate can be compared to giving and taking balls between logic gates as Fig. 1 illustrates. Because energy of a flux quantum is extremely minuscule, electric power consumed and time delay energizing (power consumption multiplied by time delay energizing is equivalent to energy consumption) at a logic gate are considerably small. Furthermore, flux quanta move between gates at as fast a speed as that of light. Thus, they exhibit the property of high-speed operation like optical interconnect in making the signal transmission between gates. In fact, movement exceeding 100 GHz (100 billion counts/sec of circulation rate) has already been verified[2], and electric power consumed at each gate is as low as 100 nW. Some semiconductor transistors operate at a speed of 100 GHz and over. However, because of their large power consumption, their use has been limited to small-scale circuits such as MUX/DEMUX and there are no precedents for their application to large-scale integrated circuits. The most important factors that distinguish the SFQ circuit from other integrated circuits are its high-speed operation combined with its low power consumption. The SFQ circuit is attractive with its capability of simultaneously achieving high-speed operation exceeding 100 GHz, large-scale integration and high-density packaging.

Because the phenomenon of superconductivity appears only at an extremely low temperature, a cooling apparatus is indispensable. Most people who are not familiar with cryogenic technology are likely to associate superconductivity with the negative image of an enormous refrigerating machine. But, the recent technological progress of compact cryocoolers is remarkable. The SSPD system we have developed, which will be introduced later, contains all required devices including a cryocooler on a 19-inch rack, which works under the household 100 V AC power system without liquid helium coolant. Once switched on, it can continue to operate anywhere. In large-scale facilities such as data centers and routers of backbone networks, air conditioners to remove the heat consume nearly 50% of the total electric power used in the entire system. As a matter of course, reduction in energy efficiency while cooling the SFQ circuit is not that small. When a cryocooler is included, energy efficiency may decrease by figures of three digits. However, if the SFQ circuit is installed in large-scale facilities such as data centers and routers of backbone networks, an energy saving effect of more than one digit can be expected even if loss in energy efficiency due to cooling is taken into account.

By taking advantage of the SFQ circuit's property of operating only at a low temperature, it can be positively adapted as a signal processing circuit for a superconductivity detector which is also operable at an extremely low temperature. With the application of superconductivity technology to various detectors for signal processing, the very domain in which this particular technology is especially strong, superconductivity detectors become more functional and advanced. In Section **3** of this paper, we will discuss details about the SFQ circuit applied to an SSPD array as a signal processing circuit, which we have recently been working on.

2.2 Current situation of research and development

The SFQ circuit is being actively studied in Japan, the US and Europe. At present, the technological level is

approaching the point where an SFQ circuit with more than 10,000 Josephson junctions is operable. Although studies to implement a RF receiver at a wireless base station have been carried out in the US[3], increasing the scale of the circuit has been problematic. In Japan, the design and evaluation technology of a large-scale SFQ circuit making use of the ISTEC Nb foundry process has been being studied and developed[4][5].

The research and development of the multilayered wiring process have been promoted with the aim of creating a tool to support the design of a large-scale circuit and improving the degree of integration[6]. In this sense, the world's leading technologies for production, design and evaluation of a large-scale circuit have already been established. However, in order to realize a circuit that is more than 1,000 times the scale of existing devices, it is essential to further develop the fabrication process and improve fabrication yields. One major factor that prevents the realization of a large-scale circuit is the difficulty in circuit debugging at a low temperature. If we are able to detect where and why an error is occurring in a circuit, effective feedback can be given to the design and fabrication processes. As a result, the operable scale of a circuit will be significantly improved.

In all of the ongoing SFQ circuit studies conducted in Japan, the US and Europe, Nb is employed as a superconductivity substance, of which the superconductivity transition temperature (*Tc*) is 9.5 K. In our lab, however, we are carrying out the research and development of an SFQ circuit using NbN with a *Tc* of 16 K[7]. Figure 2 shows a photomicrograph of the NbN integrated circuit we are developing. The use of NbN enables us to use a cryocooler which reaches a lowest temperature of 10 K. For this reason, the cooling efficiency (rate of cooling power to input power) greatly improves in comparison with the 4 K cryocooler which is used to cool Nb elements. In large-scale systems such as routers and servers, the energy efficiency of all devices including the cryocooler is regarded as important in the end. Therefore, as the improvement of the cooling efficiency of the cryocooler can be a key to the successful implementation of the device, operability at a higher temperature is crucial. NbN excels among the substances whose property controllability, stability and reproducibility of thin film and Josephson junction have a higher *Tc* than that of Nb. In this regard, NbN can be said to be the major contender as a post-Nb superconductivity substance.

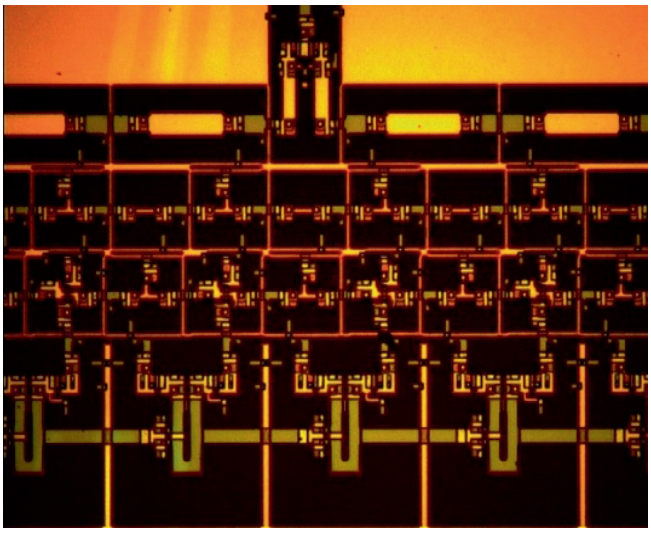

Fig. 2 Microphotograph of NbN integrated circuit

3 High-performance superconducting single-photon detector realized by SFQ signal readout

3.1 Superconducting Single-Photon Detector (SSPD)

In our lab, we are promoting the development of an SSPD using a superconducting nanowire. The SSPD is characterized by its sensitivity in a broad wavelength range extending from deep ultraviolet to mid-infrared regions. Particularly in a telecommunication wavelength of 1,550nm, it is superior to InGaAs-based avalanche photodiode (APD) as a semi-conducting material in detection efficiency, count rate, dark count rate, jitter and many other properties. For this reason, it has already been used widely in field tests of the quantum key distribution (QKD) system and quantum optics experiments[8][9]. Based on our establishment of SSPD elements fabrication technology[9] and packaging technology which secures stable coupling of optical fiber and SSPD[10], we have developed a multichannel SSPD system in which a six-channel SSPD was installed on a 0.1 W GM (Gifford McMahon) cryocooler[11]. In our system, the SSPD of all six channels exhibited a detection efficiency of 20% and higher at the dark count rate of 100. The entire system including the cryocooler can be stored on the 19-inch rack and activated by electric power of 100 V with no water cooling, making the operation convenient for use anywhere. Our SSPD system is employed in the Tokyo QKD network, which greatly contributes to the validation of system performance for the QKD network[12].

3.2 Performance improved by arrayed SSPD

The count rate of SSPD is around 100 MHz at present, which is determined by the kinetic inductance (L_K) coming from a thin and long superconducting nanowire of SSPD[13]. Because the response speed of SSPD determined by electron-phonon interaction naturally far exceeds 1 GHz, the speed can be enhanced further if the nanowire is made much shorter and L_K is further reduced. The simplest way to reduce L_K is reducing the detection area. However, because the reduced detection area decreases the fiber coupling efficiency, at least 10 μm × 10 μm of detection area is necessary. The current count rate is restricted to 100 MHz by the minimum detection area.

An effective way to reduce the nanowire length while keeping the total detection area is to divide the detection area into multiple elements[14]. High fiber coupling efficiency can be attained by arraying each pixel, while a high counting rate is achieved by minimizing the detection area of each pixel. One problem in the realization of the SSPD array is the installation in a small cryocooler. As the number of pixels increases, so does the number of coaxial cables for readout. In general, because a coaxial cable suitable for high bandwidth signal transmission is a good thermal conductor, an increase in the number of cables causes a significant rise in temperature of the cryocooler. The SSPD's performance is quite sensitive to the operating temperature and its detection efficiency deteriorates significantly with a rise in temperature. Therefore, we cannot accept a rise in the temperature of the cryocooler due to an increase in the number of cables.

3.3 SSPD output signal processing with the SFQ circuit

We propose cryogenic signal processing on the basis of the SFQ circuit [15]. Figure 3 shows its conceptual image. In this scheme, output signals sent from the SSPD array, which contains many pixels, are processed through the SFQ circuit in a cryogenic environment so that the number of output cables can be reduced substantially and the effect of thermal influx from coaxial cables can be lessened. Because the amount of heat released from the SFQ circuit is trivial, the rise in temperature of the cryocooler as a result of SFQ signal processing is negligible.

What type of signal processing circuit is appropriate depends on the intended use of the SSPD array. Figure 4 exhibits two examples of SFQ signal processing circuits. The one shown in Fig. 4(a) is a signal processing circuit which is suitable for applications requiring a high level of count rate such as a QKD system. The function of this circuit is very simple: n-channel signals from each pixel are merged into one channel. In this circuit, positional information of incident photons is lost during signal processing. When SSPD is divided into n pixels, the L_K of SSPD is reduced proportional to the number of pixels, n. Therefore, the response speed accelerates in proportion to n. The probability of each pixel being hit by photons decreases in proportion to n and this probability decrement makes it possible to realize n-fold rapidity. Eventually, the SSPD count rate improves in proportion to the square of n. For example, if the value of n is assumed to be 16, the count rate reaches a level 256 times the ongoing rate of

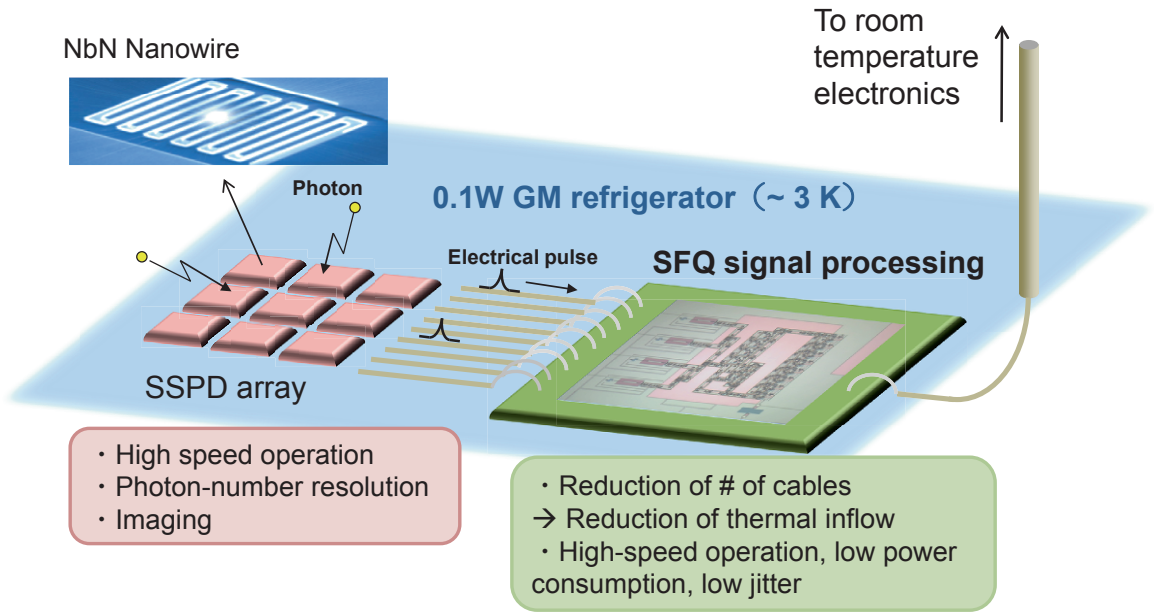

Fig. 3 SFQ signal processing for signal readout from SSPD array

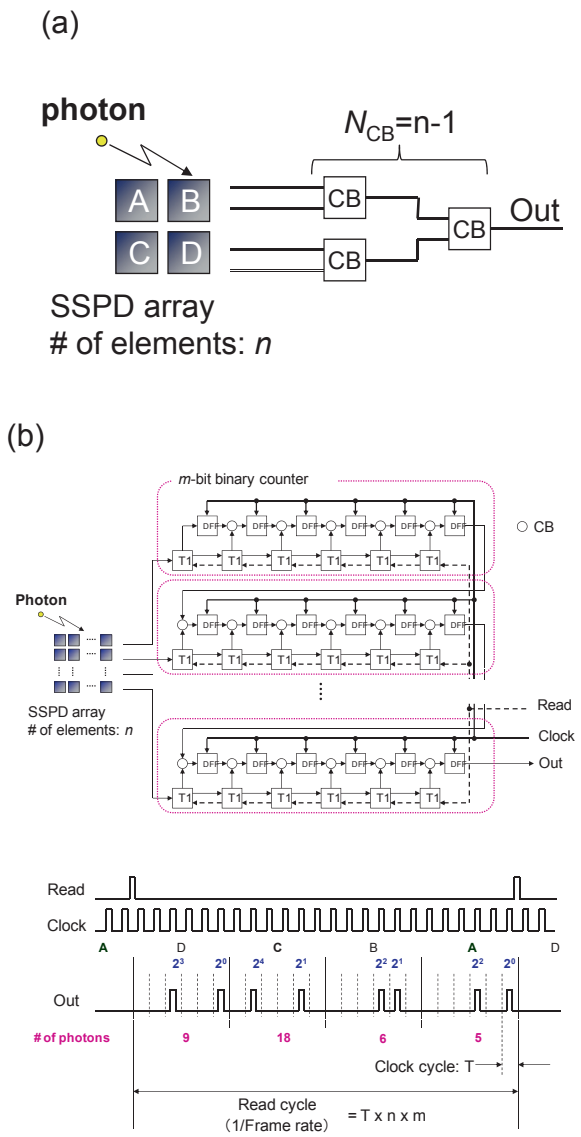

Fig. 4 Example of SFQ signal processing for SSPD array
(a) For high-speed optical communication, (b) For imaging system

100 MHz in principle. The scale of the SFQ circuit for use in signal processing is considered to produce little effect on the temperature rise of the cryocooler, as the number of Josephson junctions is less than 500 and the power consumption is less than 1 mW even on the assumption that n is 16.

Figure 4(b) shows a signal processing circuit which is assumed to be applicable to image sensors. In this scheme, a binary counter is connected to each pixel and conditions inside the counter are transmitted by external read signals to a shift register, and then the signals are read out by clock signals from the shift register in the serial. In the entire system, three high-frequency coaxial cables are required. This number of cables is unlikely to cause a significant increase in temperature in a 0.1 W GM cryocooler with a low cooling capacity. On the basis of the sequence of output signals, pixels hit by photons and the number of photon hits are identified, which makes it possible to use the SSPD array as an image sensor. Considering the scale of a circuit required for an SSPD array with 256 pixels, the number of Josephson junctions is estimated to be somewhere around 14,000, which is feasible with our current technology level. In addition, because the SFQ circuit is able to operate at a high speed, signal readout at 10 GHz and over is possible. Supposing that signals are read out of a 10,000-pixel SSPD array at 10 GHz, a frame rate of 1 MHz is feasible. If an image sensor with special qualities of high sensitivity and high-speed operation at a photon-count level is realized, it will take an active part in various fields such as biomedicine, measurement and quantum optics, contributing to the discovery of unknown phenomena and to technological innovation.

3.4 Verification of 4-pixel SSPD array performance with SFQ signal processing

We are the first in the world to have proposed the SFQ signal processing for SSPD multi-pixelization. In our past experiments, we have successfully verified the following outcomes: conversion of SSPD weak output signals of lower than 20 μA (equivalent to 1 mW or lower at a 50 Ω termination) into SFQ pulses; merger of output signals sent from two SSPDs in an SFQ signal processing circuit installed on the same cryocooler; and crosstalk-free operation through SFQ signal processing of a 4-pixel SSPD array[16]- [18]. Figure 5 indicates the experimental result of a 4-pixel SSPD array with SFQ signal processing.

Figure 5(a) is a photo showing the inside of a 0.1 W GM cryocooler equipped with a 4-pixel SSPD array and a SFQ signal processing circuit. The 4-pixel SSPD array and the SFQ signal processing circuit are connected by four high-frequency coaxial cables. As the experimental setup indicates in Fig. 5 (b), each SSPD pixel is provided with a 5 kΩ bias feed resistor on the SFQ circuit. In Figure 5(b), the SSPD and the SFQ circuit are directly connected with no bias tee. On this matter, we have already confirmed that our device operates in the same manner as in the conventional method where signals are read out of a SSPD through a bias tee and a low noise amplifier[17]. In a normal operation, after all output signals from the four channels of the SSPD array are converted into SFQ pulses and merged in the SFQ signal processing circuit to make 1-channel output signals, they are further converted by a voltage driver into square wave outputs (because SFQ pulses are minimal signals with a pulse width of ps and a voltage

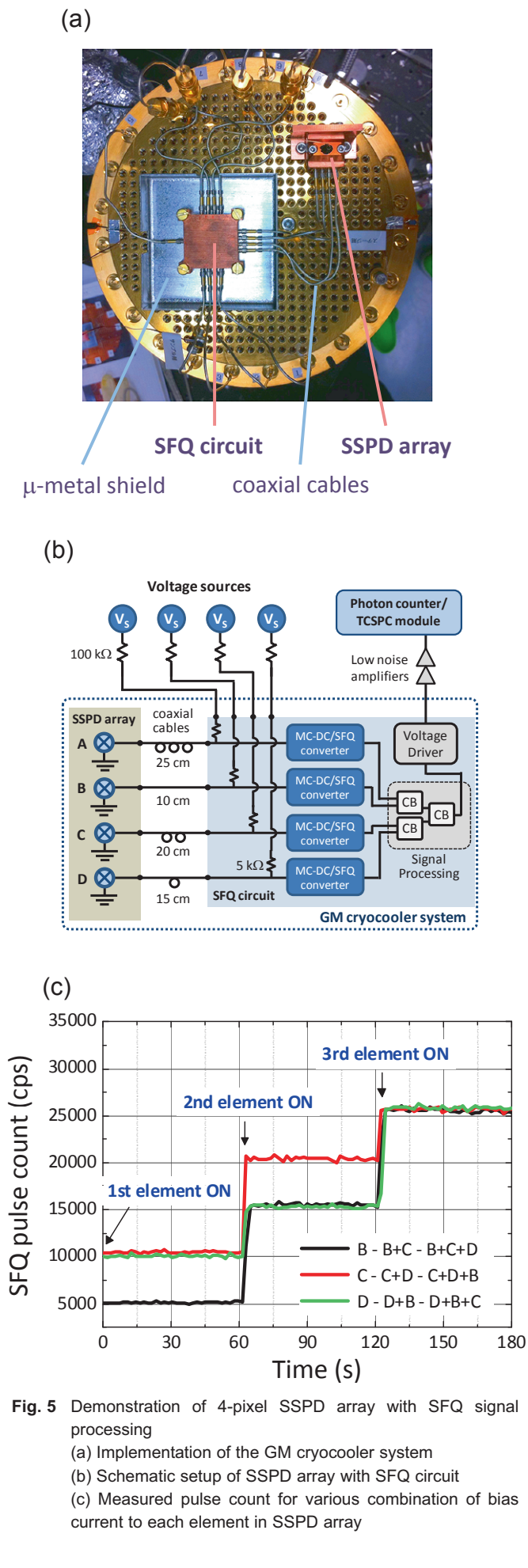

Fig. 5 Demonstration of 4-pixel SSPD array with SFQ signal processing
(a) Implementation of the GM cryocooler system
(b) Schematic setup of SSPD array with SFQ circuit
(c) Measured pulse count for various combination of bias current to each element in SSPD array

lower than 0.5 mV, they must be transformed to be read out by an external device) which can be amplified by a low noise amplifier at room temperature. Figure 5(c) indicates the observation result of the change in number of output counts, when a bias current to each pixel is turned on one by one after a bias current is adjusted in order for each pixel of the SSPD array to take the specified number of counts. The number of counts obtained is equal to the total of the counts set for each pixel, which proves that the 4-pixel SSPD array and the SFQ readout circuit are all operating normally.

In Figure 5(b), the length of the cables wired from the SSPD to the SFQ circuit is intentionally varied so that positional information of photon-hit pixels can be identified as time information on the basis of the time-correlated photon counting module. We have confirmed in the setup shown in Fig. 5(b) that photon incident pixels are identifiable through time information[18]. This method is very effective where both positional information and time information of photons need to be clarified. However, because an external trigger is used as a time reference signal to determine positional information, this method cannot be used for simple imaging where no time reference signal is obtained. For imaging only with positional information, a signal processing circuit as mentioned above and shown in Fig. 4(b) is needed.

In this verification experiment, the SSPD array and the SFQ signal processing circuit are connected by coaxial cables, which may become a problem if multi-pixelization is scaled up further. We are currently carrying on our studies in order to integrate the SSPD array and the SFQ circuit on the same substrate.

3.5 Verification of low-jitter signal readout with the SFQ circuit

Another advantage of using the SFQ circuit to read out SSPD signals is the operation of signal readout carried out in low-jitter. In case of signal readout using a normal low-noise amplifier, as the bias current to the SSPD falls, the S/N ratio of output signals deteriorates and the degree of jitter increases. The tendency of jitter increase along with deteriorating S/N ratio is also recognized when the SFQ circuit is used to read out signals. However, because the SFQ readout circuit is highly sensitive to the input current, signals are read out in low-jitter even if the output current from the SSPD is lower than 20 μA[19]. Furthermore, the degree of jitter in the SFQ circuit itself is as low as an order of a few ps. Therefore, an increasing degree of jitter in a

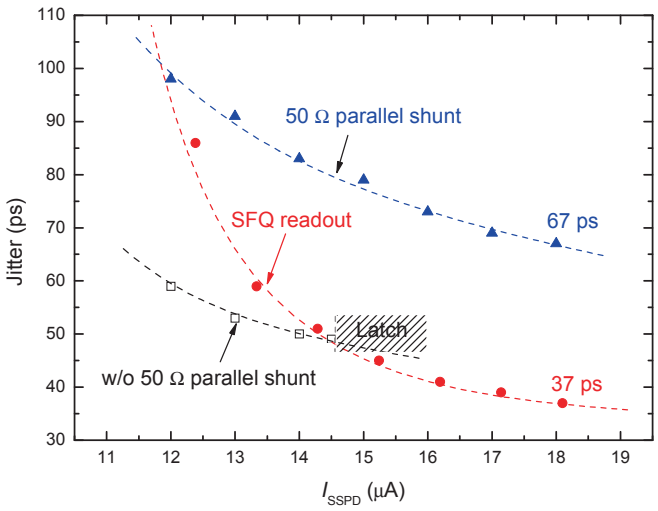

Fig. 6 Demonstration of low-jitter SFQ signal readout from SSPD

signal processing circuit can be neglected. Figure 6 shows the comparison between the SFQ circuit and the normal low noise amplifier in degree of jitter produced during readout operations.

In the normal readout method, a bias current is provided for the SSPD through a bias tee. In this situation, a phenomenon called latch-up occasionally occurs in a high bias area, where recovery from resistance is retarded due to photon incidence and thermal runaway takes place. Connecting a 50 Ω resistor parallel to the SSPD is an effective measure for preventing this latch-up phenomenon. Once the SSPD falls into the state of thermal runaway, a capacitor of a bias tee blocks the passage of DC bias, which finds nowhere but the SSPD to flow into, obstructing the recovery from the state of thermal runaway. When a 50 Ω parallel resistor is connected, it provides DC bias with an escape route, helping the recovery from thermal runaway. The effect of this parallel shunt is apparent in Fig. 6. Without a 50 Ω parallel shunt, the SSPD falls into a state of latch-up under a bias current of 14.5 μA and over. By contrast, with a 50 Ω parallel shunt connected, the SSPD operates under a bias current up to 18 μA which is almost equal to a critical current for a nanowire. For these reasons, a 50 Ω resistor is usually connected parallel to the SSPD. In comparison with this situation, the jitter issue is significantly improved by the SFQ signal readout when the bias current is 13 μA and higher. Even if the SSPD is prevented from falling into a state of latch-up with no 50 Ω resistor connected, the SFQ signal readout produces lower jitter at an input current level of 15 μA and over. These findings prove that the SFQ circuit is substantially effective in reading out SSPD signals in low-jitter.

4 Future prospects

If we are asked what the ultimate goal of the SFQ circuit study is, we would say it is its implementation in large-scale systems such as routers and servers of backbone networks. In these large-scale systems, tens to hundreds of millions of Josephson junctions must be accumulated and installed in a cryocooler as multi-chip modules (MCM) to yield signal outputs at a higher speed. We still have a long way to go before our invention is put to practical use. While businesses attach great importance to short-term profitability, public research institutes including the National Institute of Information and Communications Technology (NICT) are required to take the initiative in leading research and development. However, this has limitations unless real products are yielded. Our SSPD-incorporated study introduced in this paper was born out of such an awareness. NICT is the world's only institute that has both SSPD and SFQ circuit technologies. We believe that our unique research and development, extending to signal processing technology, will enable us to realize the world's top quality SSPD system. On the basis of the research and development for products equipped with a superconductivity sensor, if our technology level matures to the extent that a SFQ circuit with tens of millions of elements becomes operable, we may next be able to move on to the research of a large-scale SFQ circuit system with a focus on large-sized ICT devices such as routers and servers.

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