Development of Resource Allocation Re-construction Technology (Digital Beam Former and Digital Channelizer)

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We developed a prototype of integrated onboard digital beam former (DBF)/digital channelizer for flexible beam forming and flexible channel re-allocation.

In this paper, we will describe the circuit configuration of the prototype, the performances such as flexible channel re-allocation, precision beam pointing, beam-bandwidth variableness, communication quality associated with bit number of A/D converter, and the onboard instrument mounting structure.

1 Introduction

Universal provision of secure communication channels throughout Japan, desirably by means of mobile phones universally used on a daily basis, is a great challenge. The country includes dispersed remote areas and vast Exclusive Economic Zone (EEZ) water bodies where scarcely any other means of communication is available especially in times of disaster. Against this backdrop, research on the Satellite/Terrestrial Integrated mobile Communication System (STICS)[1] has been conducted in National Institute of Information and Communications Technology (NICT), which make use of two bands (uplink and downlink) of S-band frequency (bandwidth: 30 MHz) allocated to satellite communication. This approach enables securing line-of-sight communication paths by way of geostationary satellite that are not affected by disasters on the ground.

As shown in Fig. 1, this system connects a small-power mobile phone on the ground to a geostationary satellite 36,000 km above the equator. To accommodate the smallness of mobile phone power, the satellite system requires a high-gain transmitter/receiver system, which translates into adopting large antennas and spot beams.

In view of the coverable range of a spot beam and signal gain, around 100 beams are considered necessary. Figure 2 shows an example of spot beam arrangement. A phased-array antenna with around 100 elements is scheduled to be used for spot beam formation. In such a system, a DBF (Digital Beam Former) is required to process signals received from antenna elements (identification of a specific

Fig. 1 System concept of the Satellite/Terrestrial Integrated mobile Communication System
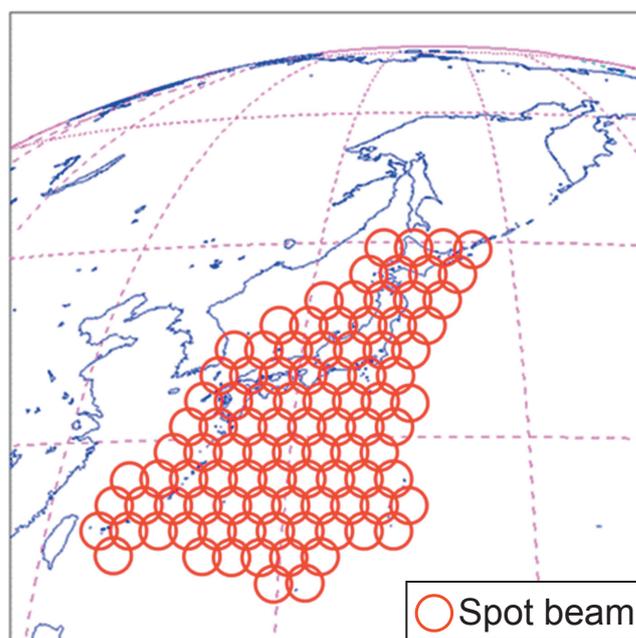
Fig. 2 Beam arrangement (an example)

beam), and to generate and transmit signals to antenna elements (beam creation)[2].

As any two adjacent spot beams must use different frequencies to avoid interference, combinatorial and repetitive use of seven frequencies is under consideration. An example of such repetitive arrangements of seven frequencies is shown in Fig. 3.

A beam is allowed to use approx. 4 MHz bandwidth if the available frequency range, 30 MHz, is split at equal intervals. Two methods are available to connect a beam to another. The one method involves beam switching on board the satellite, and the other is a two-step process: transmission of all signals to a terrestrial terminal where inter-beam connection procedures are done, followed by retransmission to the satellite where the signals are separated into each beam and are reconstructed into new frequencies. STICS uses the latter method—i.e. the beams are sent to terrestrial terminals before the beam-to-beam connection is performed. In either method, the satellite must have a function to separate signals into frequency blocks and then reorganize them. This process requires a channelizer on board the satellite capable of separating and reorganizing several thousands to several tens of thousands of blocks—depending on the frequency width for separation—and connecting to terrestrial terminals through the feeder link. Figure 4 illustrates the advantages a channelizer can endow the system with. Without a channelizer, the system transmits a wide bandwidth signal—simple addition of beams with many signal-less band frequencies interleaved in it. In contrast, the system with a channelizer can reduce the bandwidth fed to the feeder link owing to its capability to separate signals in each beam and rearrange them resulting in reduction of signal-less bands. Another advantage a channelizer can provide is the function to allocate, in times of disaster, an extraordinarily large frequency bandwidth to specific beams, whereby Resource Allocation Re-construction technology illustrated in Fig. 3 is employed. This technology takes advantage of the channelizer's variable band capability to adjust fractions of frequencies to each beam in a highly flexible fashion.

Figure 5 shows a conceptual diagram of a transponder equipped with DBFs and channelizers. The DBF/channelizer on board the satellite is required to have such provisions as: more than 100 I/O signal terminals for connecting with the user's multi-beam antenna elements and another I/O terminal with very wide bandwidth capability to connect with the feeder link. In addition, the DBF/channelizer on board the satellite must be small, light and highly power
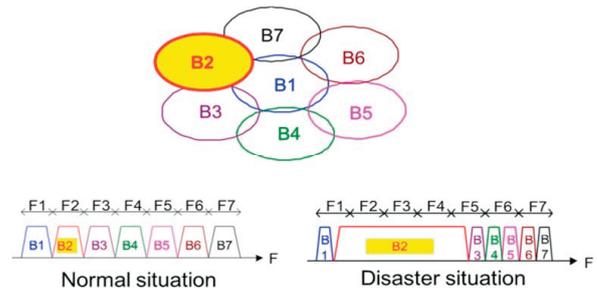
Fig. 3 An example of frequency band allocation in a normal situation and the time of disaster (7 frequencies)
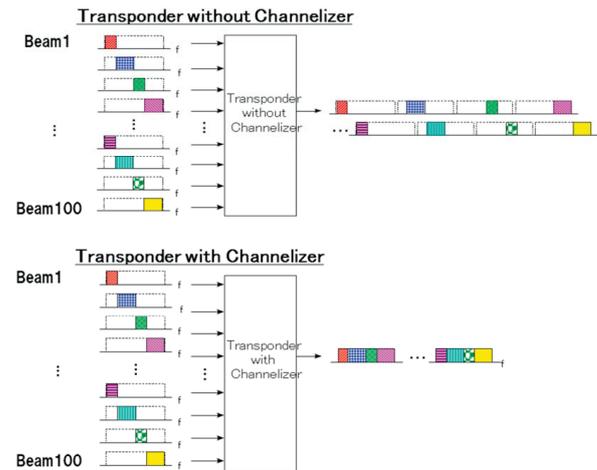
Fig. 4 Effect of efficient band utilization through the use of a channelizer

efficient. A project has been conducted in NICT to develop a prototype satellite-mounted DBF/channelizer that delivers Resource Allocation Re-construction functions in orbit[2]. In this paper, the authors describe the following aspects of prototyping the satellite-mounted DBF/channelizer: configuration and performance requirements[2], dependency evaluation of equipment performance on the bit number of its key device (i.e. A/D converter), as well as property evaluation specific to satellite-mounted equipment such as in-vacuo temperature distribution of the satellite-mounted heat dissipation system, and anti-vibration properties. Based on these results, the authors discuss the feasibility of a satellite-mounted DBF/channelizer that must operate in a harsh environment—vacuum, light weight, and severely limited power supply.

2 DBF/channelizer configuration

2.1 DBF/channelizer configuration method

There are two DBF/channelizer configuration methods available. One is to set up a DBF and channelizer mutually
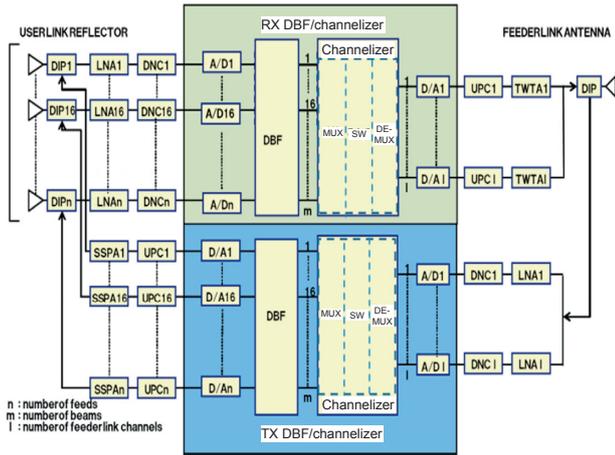
Fig. 5 Schematic diagram of a transponder equipped with DBF/channelizer

Fig. 6 DBF/channelizer individual processing configuration

Fig. 7 DBF/channelizer unified processing configuration

independently (see Fig. 6), and let them perform their tasks—beam forming and channelizing process—separately (individual processing of DBF and channelizer). The other is a three-step process (DBF/channelizer integrated processing: see Fig. 7) – the channelizer use its de-multiplexing function to split incoming signals from the antenna elements into channel units, DBF processing, and final band combining through the use of the multiplexing function of the channelizer.

2.2   Arithmetic processing in DBF/channelizer

Let us compare the two approaches in reference to the beam/channel configuration shown in Fig. 3. The DBF/channelizer individual processing configuration shown in Fig. 6 has generally larger computational load because each DBF processes all the userlink bandwidth (F1–F7 in Fig. 3) at all times to form multiple beams.

In contrast, in the DBF/channelizer unified processing approach shown in Fig. 7, each DBF processes only the bandwidth corresponding to a beam (F1 in Fig. 3) at normal times. Even in times of disaster, when the bandwidth has to be reassigned to specific areas, the arithmetic load on DBF can be reduced by implementing multiple DBFs, with each capable of processing a bandwidth narrower than that assigned to a beam (i.e. smaller channel unit). This design enables reducing wasteful arithmetic resource usage on bandwidth with scarce communication traffic.

In concreter terms, the number of multipliers, D, implemented in each Tx/Rx DBF is defined as C/fop: where C is the computational load of a DBF (multiplications/sec), and fop is the operation frequency of the multiplier. Let us
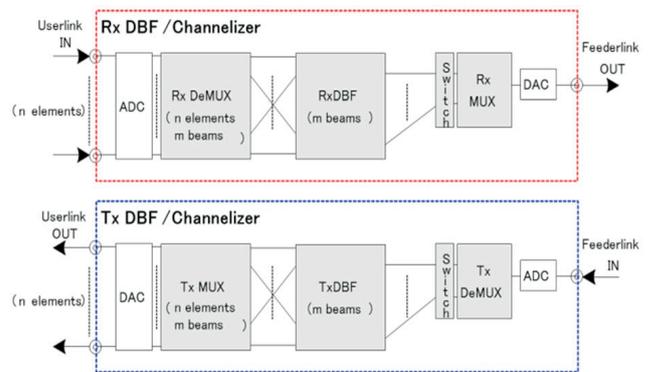
see two examples of D calculation, one for an individual processing configuration, and one for a unified processing configuration, in which the following parameters are assumed: n elements, m beams, userlink processing bandwidth 28 MHz, frequency repetitions of the userlink 7, operating frequency of the multiplier 256 MHz. Using these values, D for the DBF/channelizer of the individual processing configuration becomes $(n \times 4 \times m \times 28^*10^6$ [multiplications/sec])) / $(256^*10^6$[multiplications/sec]), and that for the unified processing configuration becomes $(n \times 4 \times m \times 28^*10^6 /7$ [multiplications/sec])/$(256^*10^6$ [multiplications/sec]) $\times 2$ (the latter calculation assumes an ideal case in which DBF processing is performed on a channel-by-channel basis).

Figure 8 shows the numbers of multipliers plotted against three combinations of parameters (elements and beams). In both processing configurations, the number of multipliers increases linearly with that of elements and beams, and the ratio remains constant. However, the absolute number of multipliers, relative to the number of elements and beams, increases more rapidly in one processing configuration than the other. For example, to realize a DBF
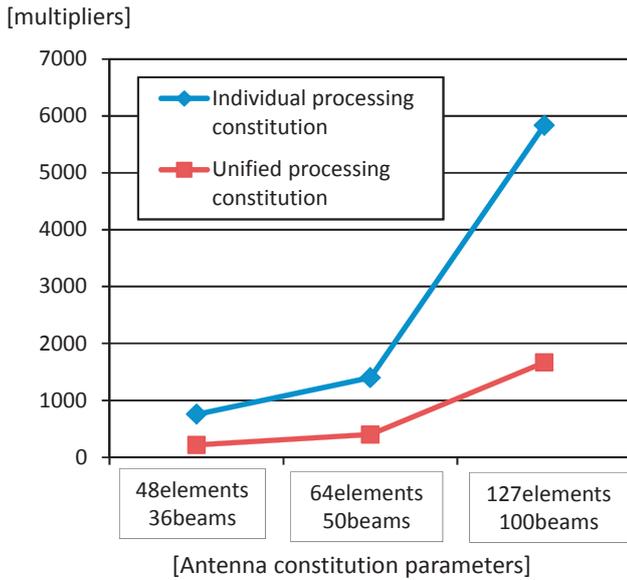
Fig. 8 Number of multipliers required to perform DBF processing vs. the number of elements and beams (an example)

Fig. 9 Transponder block diagram containing the finalized version of DBF/channelizer

that meets the specifications set by STICS—i.e. 127 elements and 100 beams—the DBF/channelizer of the individual processing configuration will require around 19 FPGAs and that of the unified processing configuration will require the much lower number of 6 (note that these calculations assume the use of space-grade FPGAs with the largest number of multipliers embedded in them).

These calculations clearly indicate that, especially for use in the multi-element and multi-beams systems envisaged in STICS, the unified processing configuration has a clear advantage to meet the requirement of satellite mounted applications—small dimensions, light weight, and low power consumption.

3 Final configuration of DBF/channelizer and prototype specifications

In view of the advantages described above, it was determined to employ the unified processing configuration (see Fig. 7) for the DBF/channelizer in this study.

To verify the feasibility of this approach, a prototype of transmitter DBF/channelizer and receiver DBF/channelizer each with 16 elements and 16 beams was developed.

The finalized system configuration of the DBF/channelizer and range of prototyping are shown in Fig. 9. A user link reflector is shown in the left part of the figure, and a feeder link reflector in the right. In the figure, the blocks in between the A/D converters ("A/D") and D/A converters ("D/A") indicate the constituting blocks of the receiver (Rx)

and transmitter (Tx) DBF/channelizers, where n and m respectively represent the number of elements and beams. Although the prototyped Tx/Rx DBF/channelizer has 16 elements and 16 beams, the final Tx/Rx DBF/channelizer system slated to be in operation on board the STICS satellite will have 100 elements and 100 beams.

In the receiver system (return system), the S-band input from the user link antenna is amplified by the amplifier (LNA), and frequency converted into the IF band by the frequency converter (DNC), and finally fed to the A/D converter in the Rx DBF/channelizer. In the DBF/channelizer, the signal is first de-multiplexed (DeMUX unit) into sub-channel units and beams are formed in DBF, followed by reconstruction of channels on the frequency axis (switching unit, SW). The signal is then multiplexed in the MUX unit before being output to the D/A converter. The signal is finally delivered to the feeder link antenna after undergoing some preparatory steps such as frequency conversion (UPC) and amplification (TWTA).

In the transmitter system (forward system), the input signal from the feeder link antenna is amplified (LNA), frequency converted into the IF band (DNC), and then fed to the A/D converter. After being delivered to the transmitter DBF/channelizer, the signal is first de-multiplexed (DeMUX) followed by reorganization of channels on the frequency axis (SW) and allocated to the desired beam for beam formation in the DBF. The beam finally undergoes multiplexing before being delivered to the D/A convertor for output. The signal is finally delivered to the user link antenna after undergoing some preparatory steps such as frequency conversion (UPC) and amplification (SSPA).

Figure 10 shows external view of the prototypes, and Table 1 lists their specifications. The user link assumes the
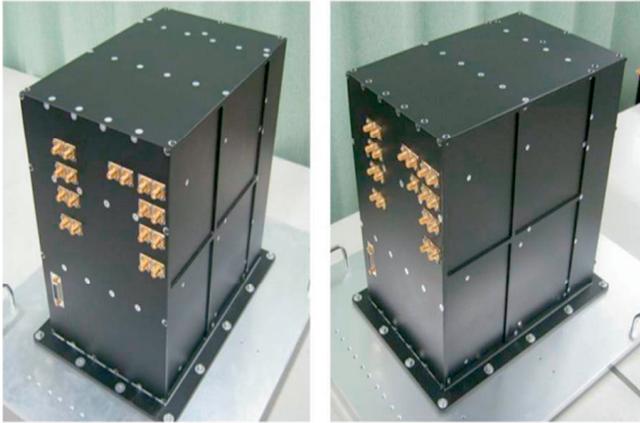
Fig. 10 External views of the prototypes: Tx DBF/channelizer and Rx DBF/channelizer

Table 1 Specifications of the prototype DBF/channelizer

Item	Specification	
	RX DBF/channelizer	TX DBF/channelizer
IN/OUT fre-quency	Input:80 MHz band 30 MHz (bandwidth) Output:1280 MHz band 200 MHz (bandwidth)	Input:1280 MHz band 200 MHz (bandwidth) Output:80 MHz band 30 MHz (bandwidth)
DBF	16 element, 16beams (procesing bandwidth 2 MHz×32 DBFs) RX DBF: with beam pointing correction function	
Chan-nelizer	DEMUX bandwidth:32 MHz DEMUX channels:256 MUX channels:2048 MUX bandwidth:256 MHz	DEMUX bandwidth:256 MHz DEMUX channels:2048 MUX channels:256 MUX bandwidth:32 MHz
	Channel interval (variable):250kHz×n (n:1~120 integer) Processing method: Bandwidth combining polyphase FFT Spectrum efficiency: $\geqq$ 90 % @1 MHzBW, ± 0.5 dB $\geqq$ 97 % @4 MHzBW, ± 0.5 dB	
A/D, D/A	Sampling frequency: 64 MHz(A/D) 1024 MHz(D/A) Quantization level: 14 bit (A/D) 12 bit (D/A)	Sampling frequency: 1024 MHz(A/D) 256 MHz(D/A) Quantization level: 12 bit (A/D) 14 bit (D/A)
Size	W180 mm×D276 mm×H300 mm	
Weight Consumed power	8.6 kg 180 W	8.1 kg 200 W

use of a 30 MHz bandwidth within S-band, which can be shared by terrestrial and satellite communications.

Computational estimate—from the number of beams and bandwidth/beam—indicates that the feeder link requires bandwidth of around 430 MHz (4.3 MHz/beam × 100 beams). Practically, in view of the limit of total transmission power available on the satellite, bandwidth of

around 100 MHz is considered to suffice (assuming a 10 kHz channel interval and 10,000 simultaneously connected lines). However, in expectation of the future capacity upgrade of satellite buses, a bandwidth larger than 200 MHz is assumed in this study. To meet the requirements from this bandwidth setting, specifications for bandwidth processing are defined as follows: 32 MHz for user link, 256 MHz for feeder link.

4　Channelizer design

Several methods are available to realize a bandwidth adjustable channelizer such as: (1) creation of several filters each with different bandwidth, from which the most desirable one is selected, and (2) partitioning of a base filter into many sub-channels, from which the one with the desired bandwidth characteristics is synthesized[3]. In this study, the method (2) is selected in consideration of its larger freedom of bandwidth variability.

The band synthesizing poly-phase FFT technique—known for its flexibility and efficient frequency utilization—is selected as the synthesizing method. This device is implemented by configuring sub-filters (consisting of registers, multipliers and adders) and an FFT circuit (see Fig. 11). This circuit is a de-multiplexing circuit in which the input signal undergoes poly-phase filtering through a plurality of juxtaposed sub-filters. Each sub-filter output is then FFT processed before being sent out to each sub-channel output.

The band-synthesizing poly-phase FFT is characterized, as shown in Fig. 11, by fine de-multiplexing into sub-channels, followed by channel-exchanging and synthesizing step. This scheme allows a high degree of freedom in synthesis bandwidth and output frequency profile settings, providing the designer with excellent flexibility.

In addition, as this method involves synthesis of outputs from many sub-channels (all with the same filtering characteristics) into a signal with desired bandwidth, the transition region of the synthesized channel's filter characteristics is the same with any one of sub-channels. Therefore, as long as the synthesized bandwidth does not fall below a certain level, efficiency of frequency utilization can be enhanced with relatively small increase in filter taps. This provides an advantage in terms of spectrum efficiency.

For synthesizing bandwidth, a filter bank is provided to create two sub-channel groups—one has the central frequency shifted by BW/2 to the other (see the operation diagram shown in Fig. 12).

In general, a larger number of de-multiplexing channels—i.e. smaller bandwidth—results in higher flexibility and spectrum efficiency, but at the cost of larger circuit size. To find an acceptable ground, the authors analyzed relations between channelizing units and the bandwidth usage ratio of the feeder link, and concluded the following specifications for channelizing at 250 kHz—user link side: 256 demultiplexing, feeder link side: 2,048 demultiplexing, and sub-channel bandwidth: 125 kHz.

Figure 13 shows a sub-channel filter characteristic of this channelizer at: cut-off frequency 0.5 T (T: symbol interval) and roll-off rate 0.5.

Assuming the sub-channel bandwidth to be BW, the transition bands at high and low regions, (1) and (2), are expressed as BW*3/8. This leads to the following equation (1) for the sub-channel filter transition bandwidth ft.

ft =(BW*3/8)*2　　　　　　　(1)

From this equation, ft at BW=125 kHz is calculated as 93.75 kHz.

The value of ft is not affected by channel synthesis: the synthesized channel's ft has the same value as the pre-synthesis sub-channels. For example, the pass-bandwidth of a 1 MHz channel is calculated as 1 MHz – ft ≒ 0.906 MHz,

indicating the theoretical feasibility of 90.6% spectrum efficiency without the occurrence of leak out of the target bandwidth. By the same token, the pass-bandwidth of a 4 MHz channel is calculated as 4 MHz – ft = 3.906 MHz (see Fig. 14), indicating the theoretical feasibility of 97.6% spectrum efficiency without the occurrence of leak out of the target bandwidth.

5　DBF design

5.1　DBF configuration

To support flexible bandwidth modifications on a beam-to-beam basis, the system implements 32 DBF circuits each with 2 MHz band processing capability (two DBF circuits process one beam equivalent of bandwidth, 4 MHz at normal times).

The prototyped DBF, with each DBF circuit capable of processing 16 elements, can control antenna beam direction. In addition, through combination with channelizers, a 16-beam bandwidth variable DBF is realized.

5.2　Beam direction control

To enhance the accuracy of the beam direction, DBF
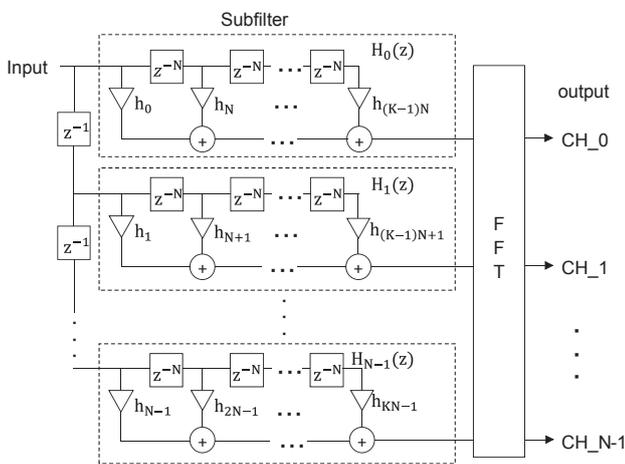
Fig. 11　Configuration of poly-phase FFT
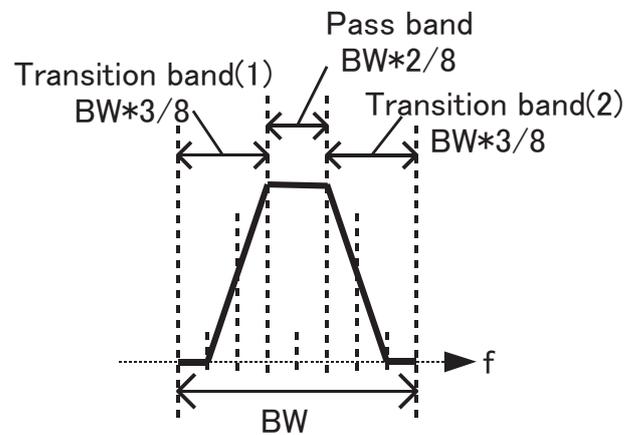
Fig. 13　Filtering characteristics of a sub-channel
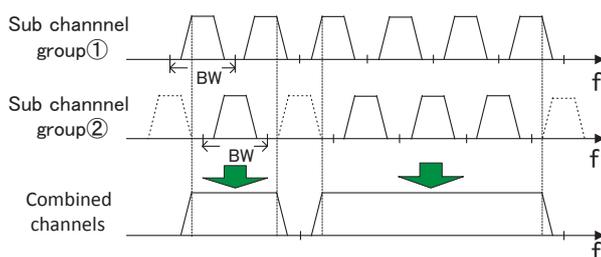
Fig. 12　Schematic representation of channelizer actions
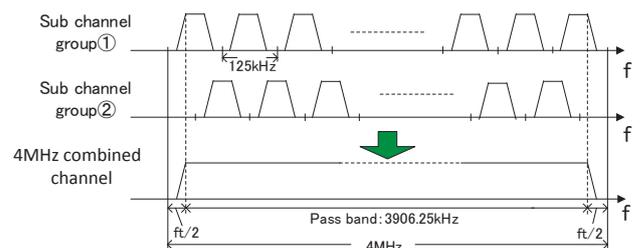
Fig. 14　Spectrum efficiency in a 4 MHz channel

feedback functions are given to the Rx DBF/channelizer, for which RF sensor calculation of beacon signals is made use of.

The objective of this function is to correct directional misalignment of the beacon signal beam—created by Rx DBF—in reference to the incident direction of the beacon signal (directional reference).

A block diagram of the DBF feedback function is shown in Fig. 15, and its control flow is shown in Fig. 16.

The beacon signal (assigned as a part of the input signal) is extracted when it enters into the Rx de-multiplexer and is delivered to the beacon signal DBF (a DBF installed inside the Rx DBF independently from the communication channel DBF, used exclusively for beacon signal process-ing). In reference to the initial DBF coefficients written in the DBF coefficient table, the beacon signal DBF performs the following RF sensor calculations: sum signal, East-West difference signal (Diff signal (AZ)), and South-North dif-ference signal (Diff signal (EL)).

The control unit (Rx Cont) detects phase polarity (code) of these three signals (sum and two differences) to deter-mine the 2-dimensional direction of correction using the algorithm shown below.

First, the phase values of the sum signal (Φa), East-West difference signal (Φdaz), and South-North difference signal (Φdel) are expressed by the following equations (2) to (4), respectively.

$$\Phi a = \tan^{-1}(Qa/Ia) \tag{2}$$
$$\Phi daz = \tan^{-1}(Qdaz/Idaz) \tag{3}$$
$$\Phi el = \tan^{-1}(Qdel/Idel) \tag{4}$$

Where, Ia is the real part of the sum signal output and Qa the imaginary part, Idaz is the real part of the East-West difference signal and Qdaz the imaginary part, and, Idel is the real part of the South-North difference signal and Qdel the imaginary part.

Next, polarity comparison is made between Φa and Φdaz, and between Φa and Φdel. If each comparison shows coincidence (i.e. in-phase), then the corrective direction points in the negative (-) direction. If they do not coincide (i.e. out-of-phase), then the corrective direction points in the positive (+) direction.

In addition to the corrective direction as determined above, a pre-determined corrective step value, information of elements arrangement, signal frequency, and antenna parameters (installment of reflector, and others) are used to calculate the correct function for each DBF coefficient
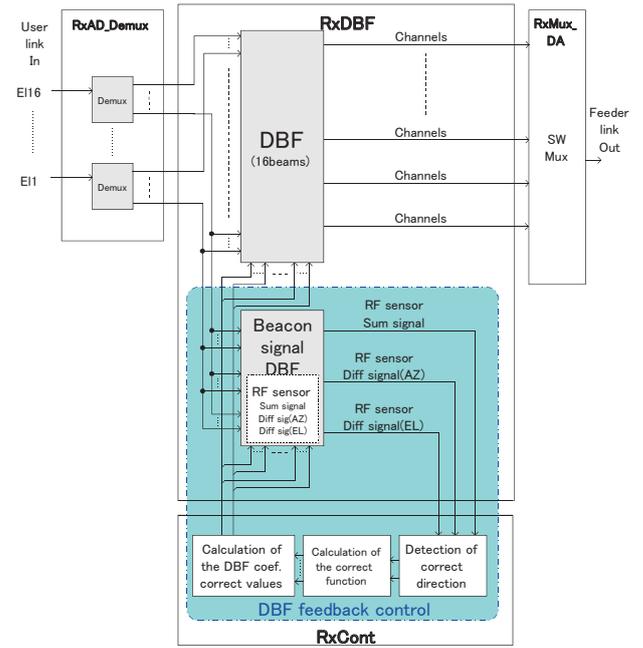
Fig. 15 Block diagram of DBF feedback function
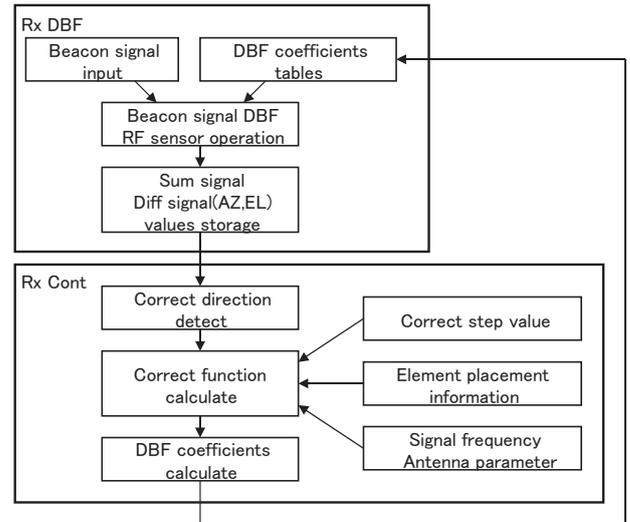
Fig. 16 Flow chart of beam direction control

of each DBF element. DBF coefficient tables of each beam are modified reflecting these sets of corrective information. The steps described above are repeated to correct the beam direction.

6 Results from prototype evaluation

6.1 Channelizer characteristics

Channelizer characteristics of the Rx and Tx DBF/channelizer were measured, and the results satisfied the

required performance in terms of spectrum efficiency and feeder link I/O bandwidth.

Figure 17 shows a result from de-multiplexing/multiplexing simulations. Figure 18 shows channelizer characteristics obtained from the Tx DBF/channelizer. Table 2 shows the results of spectrum frequency measurements and feeder link I/O bandwidth measurements.

The results from experimental measurements are in close agreement with those from the simulations, indicating that the prototype meets the performance requirements in terms of spectrum efficiency and feeder link I/O bandwidth.

As seen from the filter characteristics plots, steep edges are commonly observed irrespective of the target channel bandwidth, which is a typical characteristic of the band synthesizing poly-phase FFT method.

Figure 19 is a diagram illustrating an example of bandwidth allocation: 4 MHz, 8 MHz, 16 MHz, and 25 MHz

are allocated to B2. Figure 20 shows the experimental results corresponding to each of these allocations. Note that different signal levels are fed in each experiment to distinguish waveforms clearly. The plots clearly indicate that the allocated bandwidths are in good agreement with the expected values.

6.2 Correction of beam direction (Rx DBF/channelizer)

The following experiment was conducted without using a reflector to verify the effectiveness of the DBF feedback function imparted to the Rx DBF/channelizer. First, initial

Table 2 Spectrum efficiency of prototype channelizer

Item		Result	Note
Spectrum efficiency	1 MHz / channel	91%	Bandwidth(0.5dBpp) 0.91 MHz
	4 MHz / channel	97.5%	Bandwidth(0.5dBpp) 3.9 MHz
Feeder link bandwidth		≥200 MHz	

Fig. 17 Simulated de-multiplexing/multiplexing characteristics of channelizer
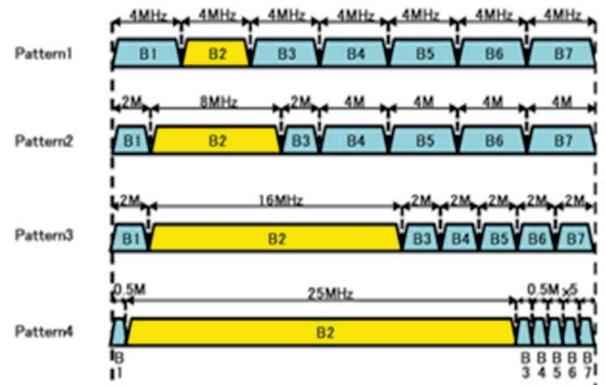
Fig. 19 Frequency band allocation to 7 beams (an example)

Fig. 18 Experimentally measured de-multiplexing/multiplexing characteristics of channelizer
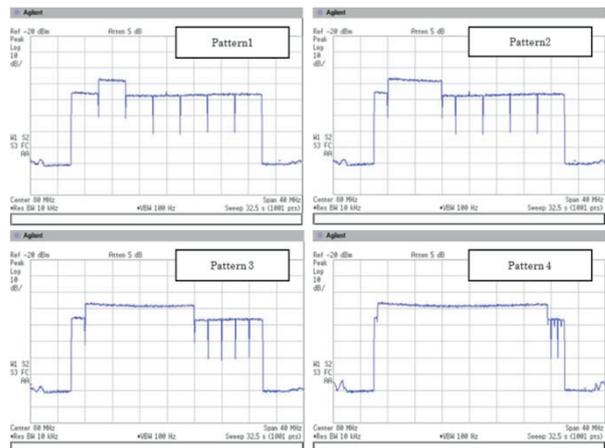
Fig. 20 Frequency band allocation to 7 beams (experiment results)

coefficient values for sum, East-West difference, and South-North difference are set to both the beacon signal DBF and communication channel DBF (note that the East-West and South-North coefficients have an offset of 10 degrees in the positive direction). Then, a corrective process is started with the beacon signal (CW) incident from the frontal direction (0 deg). Under this condition, pre- and post-correction signal levels of the following signals were measured—sum, East-West difference, and South-North difference.

To enable simultaneous monitoring of the three output signals—sum, difference (East-West) and difference (South-North)— they are positioned at different frequencies on the feeder link band using a channelizer function.

Figure 21 shows the results obtained from the beam direction control experiment. The frequencies 1, 2 and 3 correspond respectively to the three output signals—sum, difference (East-West) and difference (South-North). Comparison of pre- and post-correction signals revealed that the correction enhanced the output level of sum signal ($\geqq$9 dB), but decreased the output level of the two difference signals by a magnitude of no less than 30 dB. These are exactly the expected results. Table 3 summarizes results of the beam direction controllability experiment in numerical terms. These results clearly indicates that the DBF/channelizer's beam correction function of our development performs very effectively, offering promise to realize multi-beam direction control in STICS.

6.3 How the number of bits of the Rx A/D converter affects system performance

6.3.1 Characteristics of the Rx A/D converter

The Rx DBF/channelizer's input unit requires the deployment of a large number of A/D converters—more than 100, each corresponding to an antenna element. A/D converters for space use with exceptional environment resistance (radiation, temperature) tend to consume large power, and the power consumption become even larger as its bandwidth increases (0.5 to several Watts per device). Higher resolution (or, larger number of bits) generally translates into higher system performance, often at the cost of increased power consumption. In view of power usage considerations, the number of bits of A/D converters should be reduced as far as the other conditions permit. The authors conducted experiments to verify the effect of bit numbers on system performance.

Figure 22 shows the measured A/D converter I/O characteristics for the number of bits 6, 8, 10, 12 and 14.
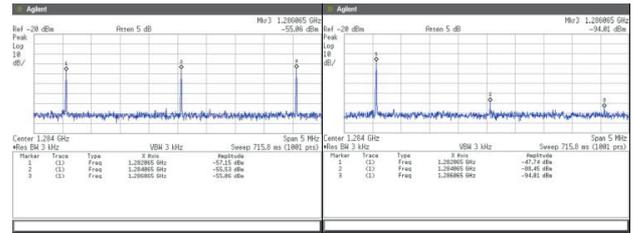
pre − correction　　　　　　post − correction

Fig. 21 Results of beam direction control experiments

Table 3 Summarized results of beam direction control experiments

Signal	Sum signal	Difference signal (East-West)	Difference signal (North-South)
Before correction	–9.5 dB	–7.8 dB	–7.4 dB
After correction	0 dB	–40.8 dB	–46.3 dB
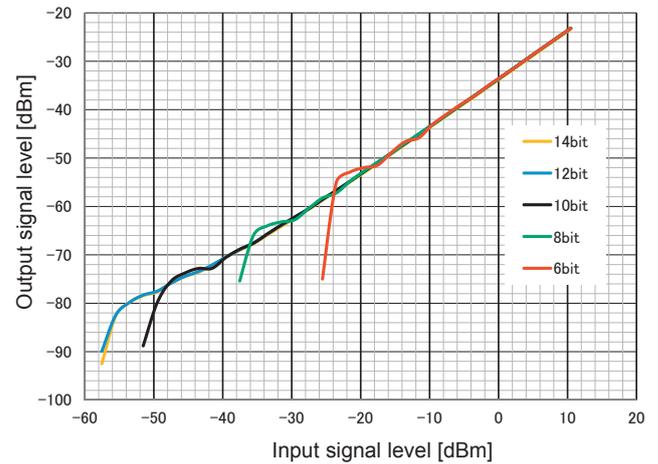
Fig. 22 I/O characteristics dependency on the bit number of the A/D converter

Lower limits for three smaller-bits cases (6, 8 and 10 bits) exhibited approximately 12dB intervals (6 dB per bit). For the two large-bits case (12 and 14 bits), lower limits are not clearly distinguishable, presumably because of system noise interference.

6.3.2 Evaluation by bit error measurement

A modulation signal and band-limited noise were input into the receiving terminal of the Rx DBF/channelizer, and the output signal from the channelizer was demodulated for bit error rate (BER) measurement. The bit number of the A/D converter was used as the experiment parameter. Parameters used to run the BER characterization test are listed in Table 4, and a block diagram of the test setup is shown in Fig. 23.

BER characteristics for each A/D converter bit number

of the DBF/channelizer are plotted in Fig. 24 (Eb/N0 = 10 dB for all plots). For three low bit number cases (6, 8 and 10 bits), BER starts to deteriorate significantly at distinctively separated regions—the interval between them was roughly 12 dB (approx. 6 dB per bit). Such differences are not clearly distinguishable for two large bit number cases (12 and 14 bits), but the plots indicate measurable differences in dynamic range.

6.3.3 Evaluation by EVM

To evaluate the effect of bit number of A/D converters on dynamic range more closely, the Error Vector Magnitude (EVM) method was used, which essentially examines the ratio between the ideal vector and error vector.

The EVM evaluation formula, (5), is shown below. Figure 25 shows a screenshot during the EVM measurement.

$$\text{EVM}[\%] = \frac{|E|}{|V|} \times 100 \tag{5}$$

Figure 26 shows the results of EVM characteristics measurements, in which the bit number of the A/D converter is used as the parameter. For lower bit number cases (6, 8 and 10 bits), EVM starts to deteriorate at three distinctively different input signal levels, and the interval between them is approximately 12 dB (or, 6 dB per bit). Such differences are not clearly distinguishable for two large bit number cases (12 and 14 bits). However, the plots indicate measurable differences in dynamic range, indicating the need to use a bit number no smaller than 12 bits.

Table 4   Parameters used to run BER characterization test

Item	Condition
A/D quantization level	14,12,10,8,6
Modulation scheme	QPSK
Transmission rate	1 Mbps
Filter	Root Nyquist
Roll-off factor	0.5
Noise bandwidth	30 MHz
Eb/No	10 dB

Fig. 23   Block diagram of BER characterization test
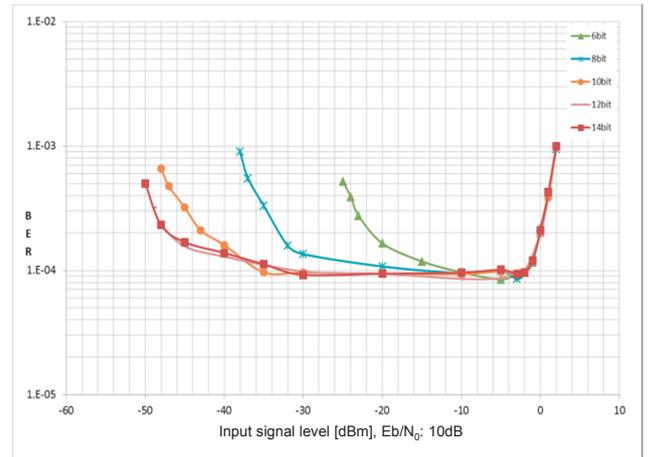
Fig. 24   BER characteristics of the DBF/channelizer at Eb/N_0 =10 dB (each plot corresponds to an A/D converter bit number)
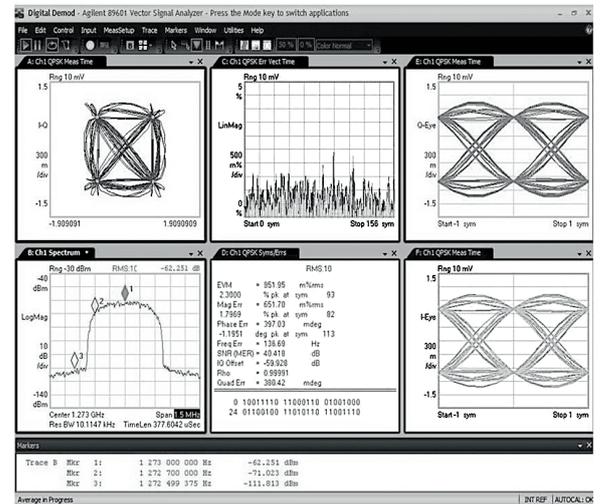
Fig. 25   A screenshot during EVM measurement
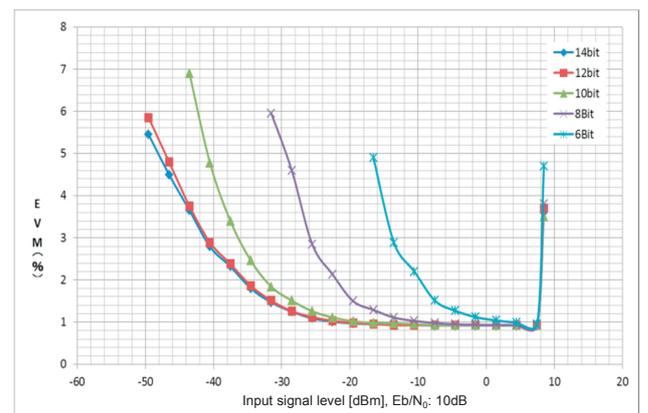
Fig. 26   EVM characteristics (each plot corresponds to an A/D converter bit number)

7   Mountability examination

7.1   Heat dissipation structure

The DBF/channelizer is considered to emit heat nearly equivalent to its power consumption—i.e. 2600W (see Section **7.2** below). Major heat sources are almost exclusively A/D converters and FPGAs, and examination of heat dissipation structures involving these devices is a prerequisite for proper review of mountability. The authors examined heat dissipating structures using an assembly consisting of four PC boards (slices) shown in Fig. 27. Each PC board is mounted with four FPGAs. Heat emitted from the on-board FPGA is conducted to the base of the PC board by means of a heat pipe. The design assumes the power consumption of a FPGA (heat source) to be 20 W (80 W per PC board), and the temperature of the mounting surface to be 53℃.

Prior to actual measurements in a thermal vacuum test,

thermal analysis simulation was conducted to predict temperature distribution (Fig. 28). Measurements were taken from selected points on slice A that represent the flow of heat—connections to heat source (2, 3, 6 and 7), connections to heat sink (8 and 9) and the center of the PC board (5). The data obtained from this thermal vacuum test and the results of analysis are summarized in Table 5. The measured values showed good agreement with the results of thermal analysis. From the measured data, the temperature at the upper junction to heat emitting body ② is 8.6℃ higher than that at the junction to heat sink ⑨. Similarly, the temperature at lower junction ⑥ is 3.3℃ higher than that at ⑧. From these data, we can confirm that the use of a heat pipe system enables implementation of four high-heat-generating 20 W class FPGAs on a PC board (20 W) at the cost of temperature rise not exceeding 9℃ between the heat emitting body junction and heat sink junction.

In the tested assembly, the heat pipe is laid out directly on the surface of the PC board. This heat conducting system structure was tested to make sure it meets vibration resistance requirements for mounting on a satellite. Figure 29 shows the vibration test arrangement. Thumping

Fig. 27 Assembly for simulating heat dissipation structure (measurement points are numbered)

Table 5 Simulated and measured temperatures

Measuring point	Measured temperature	Analyzed temperature	Difference
No.2	72.7℃	72.2℃	–0.5℃
No.3	71.2℃	72.0℃	+0.8℃
No.5	81.5℃	79.9℃	–1.6℃
No.6	68.4℃	68.7℃	+0.3℃
No.7	71.0℃	68.5℃	–2.5℃
No.8	65.1℃	63.3℃	–1.8℃
No.9	64.1℃	61.8℃	–2.3℃
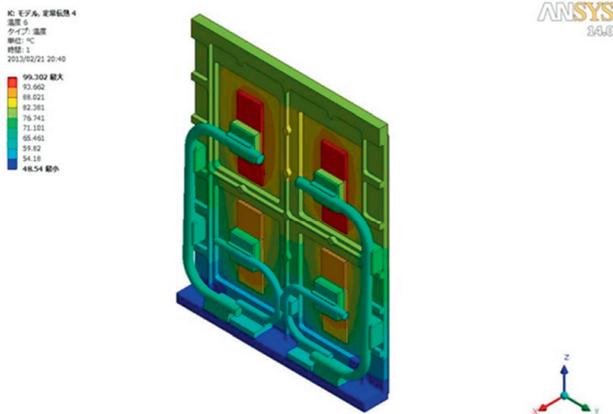
Fig. 28 Heat dissipation structure and temperature simulation
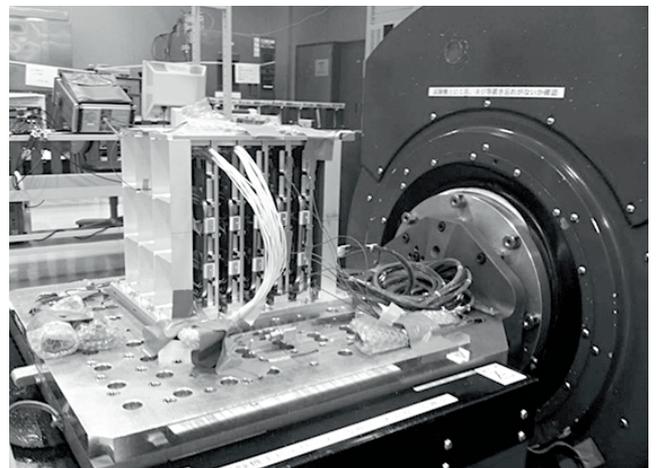
Fig. 29 Evaluation through vibration test

vibration that simulates satellite launching was inflicted on the assembly, and no significant problem was detected.

7.2 Power consumption and mass of satellite mounted DBF/channelizer, and resource allocation in a satellite

Based on the results gained from the Tx and Rx DBF/channelizer prototypes (16 elements and 16 beams), an analysis was made to estimate the power consumption and mass of the final full scale DBF/channelizer (127 elements and 100 beams) to be implemented in STICS. Table 6 summarizes the analysis results.

The satellite planned in STICS will have a launching mass of about 6 tons accommodating such units as a large reflector antenna (diameter of mechanical aperture approx. 30m) and Rx- and Tx-DBF/channelizer (capable of supporting 127 elements and 100 beams). Typical resource allocation for such a satellite is summarized in Table 7. In terms of mass, the Tx-, Rx-DBF/channelizer has attained an acceptable level for mounting on the satellite. However, power consumption still needs reduction. In view of the fact that the FPGAs inside the DBF/channelizer consume the major portion (approx. 70%) of the electric power, focused efforts should be made toward reduction of power consumption in FPGAs. To achieve this goal, specifications for a satellite mountable DBF/channelizer must be defined based on surveys and feasibility examinations on such subjects as: scaling down of circuitry (optimized system/

Table 6 Estimated power consumption and mass of a satellite-mounted DBF/channelizer

Item	Tx DBF/channelizer	Rx DBF/channelizer	Total
Power consumption	1400 W	1200 W	2600 W
Weight	~74 kg	~70 kg	~144 kg

Table 7 Resource allocation plan for a satellite

Item	Weight (kg)		Power consumption (W)	
Communication payload	1,530		10,700	
	· Large antenna	290	· Large antenna	0
	· DBF/channelizer	200	· DBF/channelizer	1,300
	· SSPA	160	· SSPA	7,090
	· TWTA	50	· TWTA	1430
	· Others	830	· Others	880
Satellite bus	1,500		2,400	
	Propellant			
	2,800			
Total	5,830		13,100	

circuit configuration), availability of highly integrated low-power devices (e.g. development of ASICs), and review of performance requirements.

8 Conclusions

In this paper, the authors give an account of the prototype development of the satellite-mounted DBF/channelizer (configuration and performance items), to which they have been engaged as a part of the STICS project. Discussions in this report also include such subjects as: evaluation of the effect of A/D converter resolution (number of bits) on system performance, evaluation of temperature distribution in the heat dissipation system under vacuum (in view of future use in space), and experimental evaluation of anti-vibration properties. Based on these data, the authors discuss the feasibilities of satellite-mounted DBF/channelizers.

Based on the results gained from the prototype's performance evaluations, the authors could confirm the following essential items: the channelizer is capable of de-multiplexing, multiplexing, and reconfiguring signals in a very flexible way; the beam direction correction function is capable of automated execution; the variable beam bandwidth function allows concentrated allocation of frequency bands to a specific beam when the need arises (e.g. in a time of disaster). A/D converters—one of the major devices—are implemented in great number in a DBF/channelizer and exert a huge impact in terms of power consumption and system performance. The authors evaluated the effect of an A/D converter's bit number on system performance, and concluded that 12- to 14-bit resolution is required. The authors examined mountability of DBF/channelizers on a satellite, especially from the viewpoint of heat dissipating structures. Thermal vacuum tests and vibration tests were conducted on electronics assembly consisting of multiple PC boards (heat pipes mounted on it to draw heat from the ICs). The data gained from these tests—temperature distribution, anti-vibration properties—contributes to expanding our knowledge in view of constructing satellite-mounted structures.

These results contribute to establishing basic technologies for the realization of a satellite-mounted DBF/channelizer.

In terms of mass, our results meet the objectives set by the resource allocation plan for satellite construction. In terms of power consumption, however, further reduction efforts are needed. The authors are planning to extend their

research for lower power consumption and better satellite-mountability to define a roadmap toward realization.

9　Acknowledgments

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